

Silverton / SilverOak

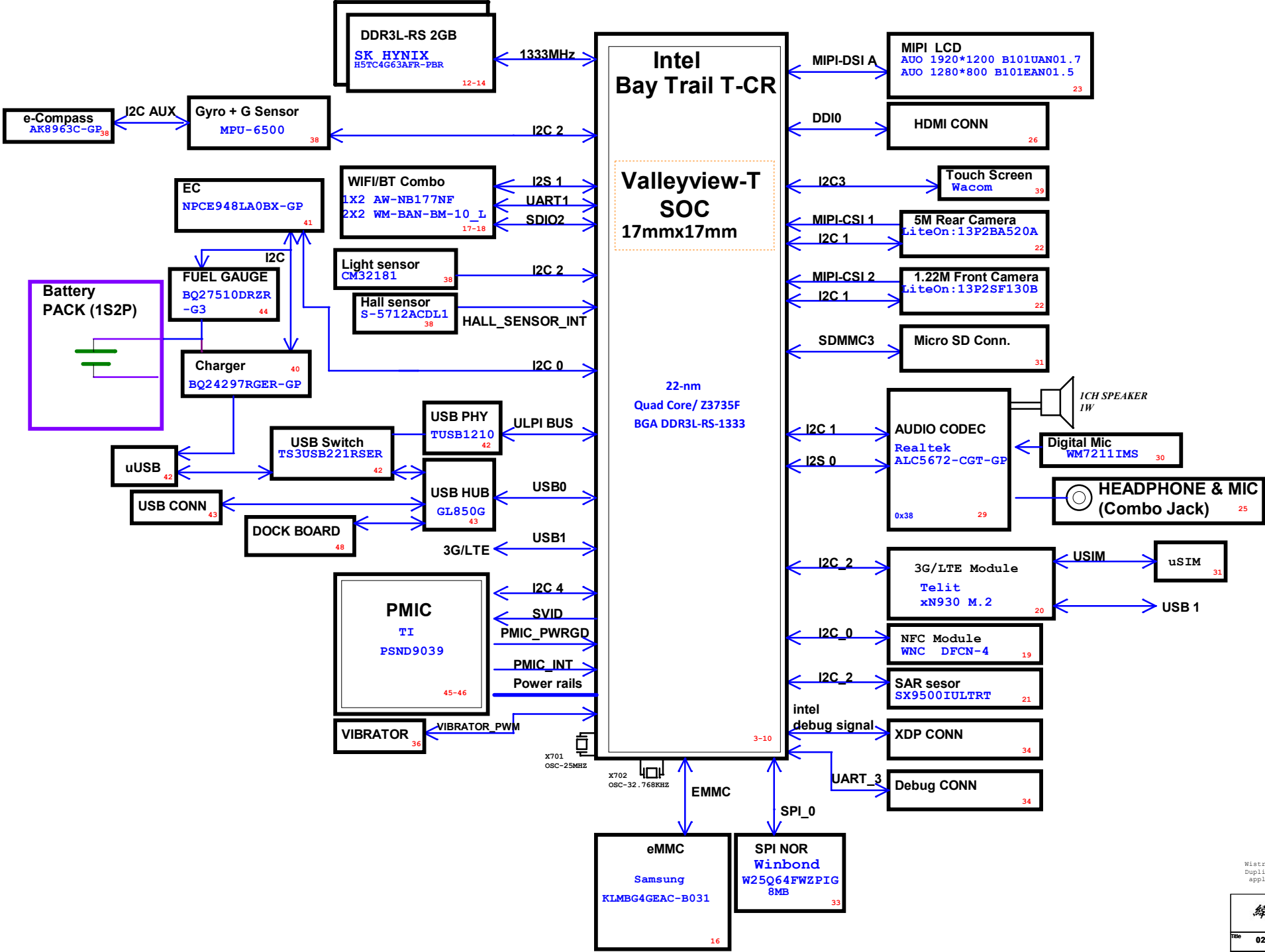
2014-12-09

REV : 0 (X-build)

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Title 01_Cover			
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# Block Diagram



System Power PMIC PSND9039	
INPUTS	OUTPUTS
+VSYS	+V_VNN +V_VCC +VDDQ +V1P0SX +V1P0A +V1P8A +V3P3A_PMIC +V2P85S +VRTC +AVDD_CAM +V1P8_Rear V1P8SX_2 +V3P3A_TP +VSUDIO +VSD +V3P3A LCM_VDD_3V3
+V1P8A	+V1P2Sx +V1P2A
RT9040GQW-2-GP	
INPUTS	OUTPUTS
+VDDQ	+VDDQ_VTT
CHARGER BQ24297	
INPUTS	OUTPUTS
5V / VBAT	+VSYS
5V BOOST SY7066QMC-GP	
INPUTS	OUTPUTS
+VSYS	+V5P0_BOOST
3V3 BUCK SY8010ZDEC-GP	
INPUTS	OUTPUTS
+VSYS	+3V3_A
PCB LAYER LDI 8L	
L1:Top L2:GND L3:Signal L4:GND	L5:Signal L6:Signal L7:GND L8:Bottom

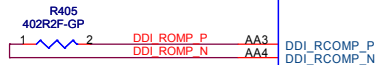
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Title			
03_CPU (LPDDR3)			
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# SOC : DDI 0&1 / MIPI-DIS/MIPI-CSI/MIPI-GPIO

## HDMI

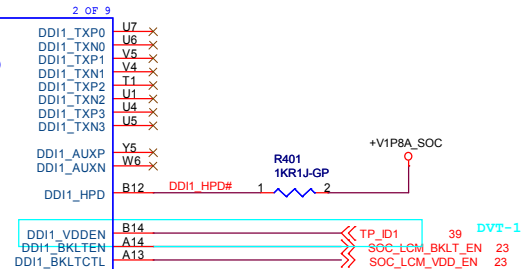


## MIPI Display



VALLEYVIEW-T-2-GP

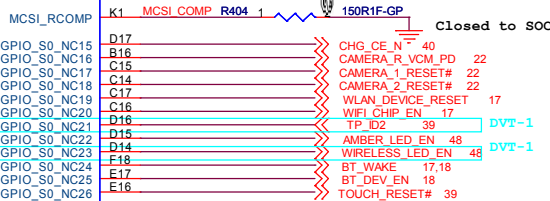
## eDP



## Rear Camera



## Front Camera



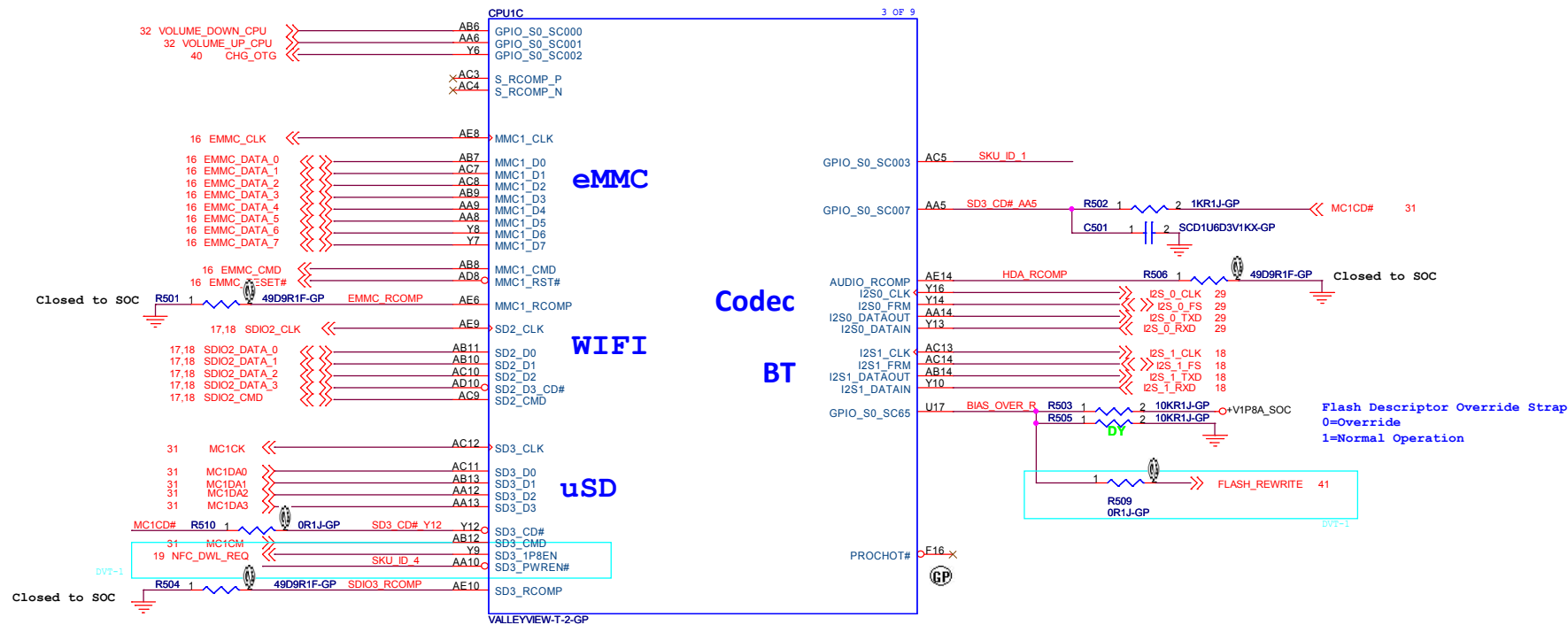
Ball Map	GPIO	Customer Name	Function
A14	GPIONC10	DDI1_BKLTEN	MIPI_BKLT_EN
A13	GPIONC11	DDI1_BKLTCTL	MIPI_PAENL_EN
AA16	SIO_PWM/GPIOC_94	SIO_PWM[0]	MIPI_BKLT_CTRL
B14	GPIONC9	DDI1_VDDEN	MIPI RESET

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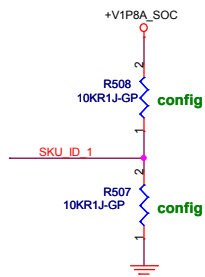
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Title 04_CPU (eDP/HDMI/MIPI)		
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# SOC : eMMC/SD/GPIO/I2S

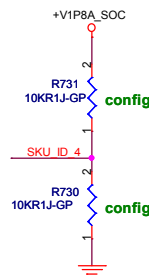


**NFC ID (GPIOC\_3)**  
H: with NFC  
L: without NFC



DVT-2

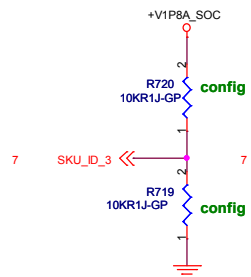
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L: without WWAN



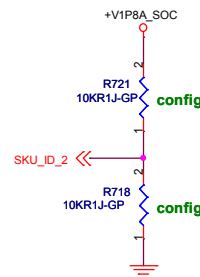
DVT-2

**EMMC ID1**  
GPIOC\_74

**EMMC ID2**  
GPIOC\_75



DVT-2



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Title **05\_CPU (SD/eMMC/AUDIO)**

Size A3 Document Number **SILVERTON/SILVEROAK**

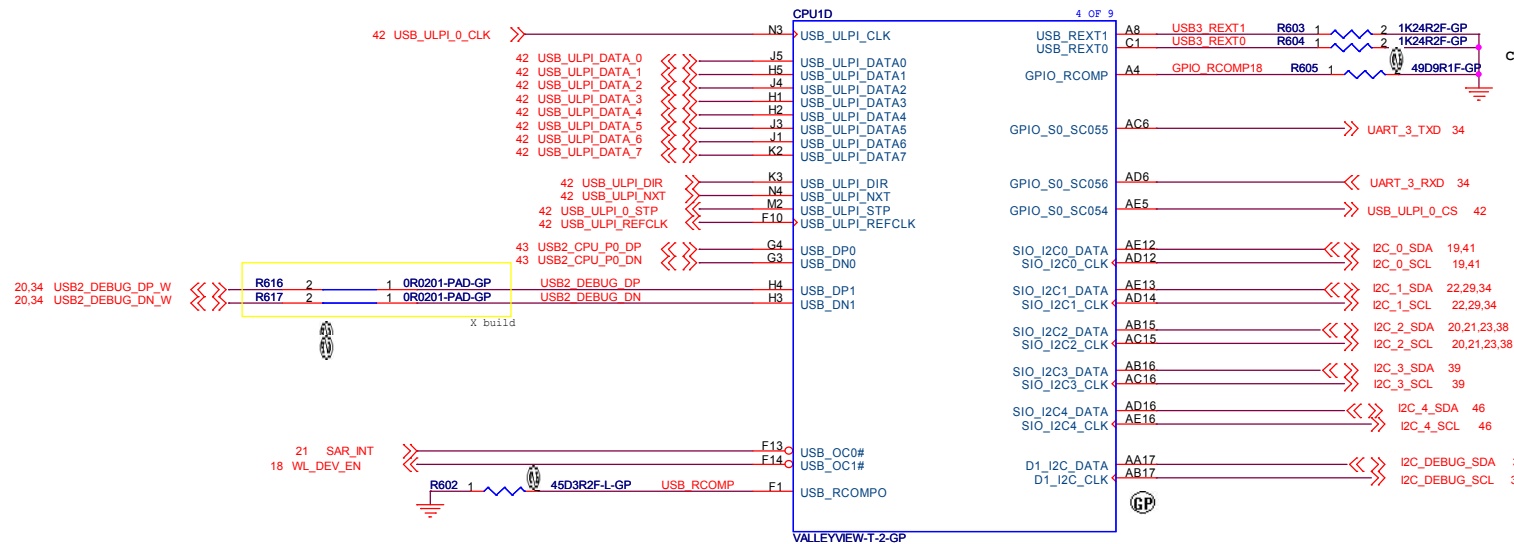
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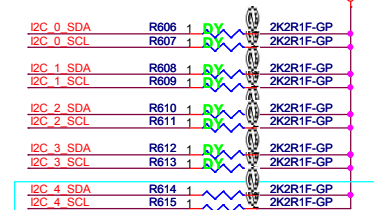
Function	GPIO	16G	32G	64G
EMMC_ID1	GPIOC_74	1	0	1
EMMC_ID2	GPIOC_75	0	1	1

# SOC : USB/ULPI/HSIC/LPC/SMBUS/HSI/I2C



Closed to SOC

below reserved



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Title 06_CPU (USB/HSIC/LPC/HIS/I2C)			
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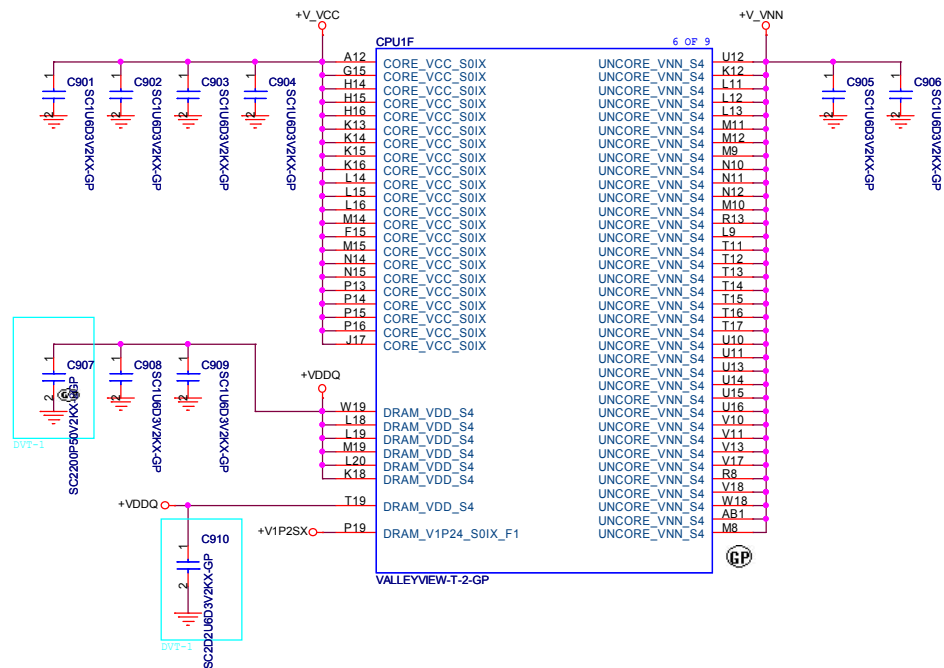
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08_CPU (VCCIO)			
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# SOC : VCC/VNN

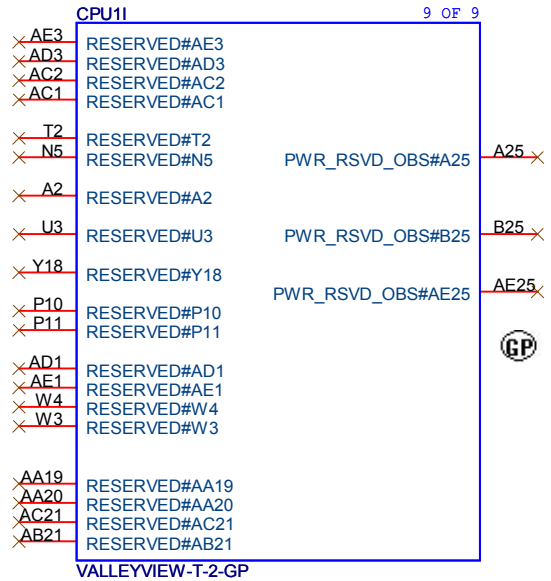
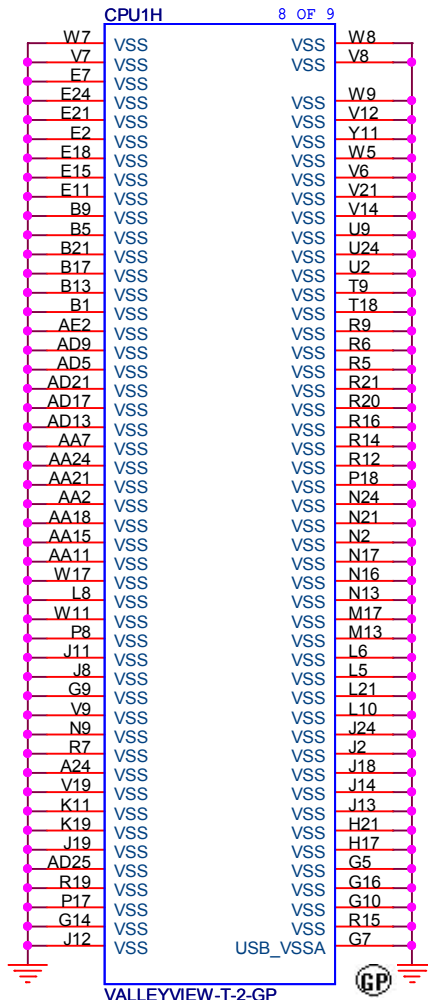


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09_CPU (VCC/VNN)		
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SOC : GROUND



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Title

10\_CPU (VSS)

Size

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SOC DECOUPLING

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Title

11\_CPU (VLV2 Decoupling)

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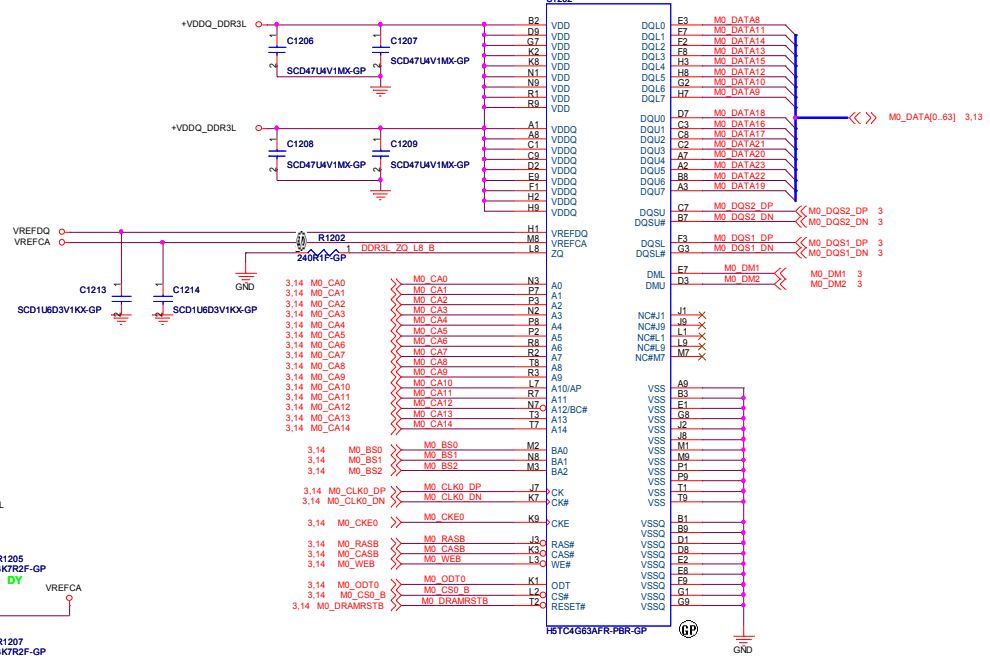
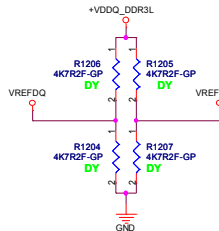
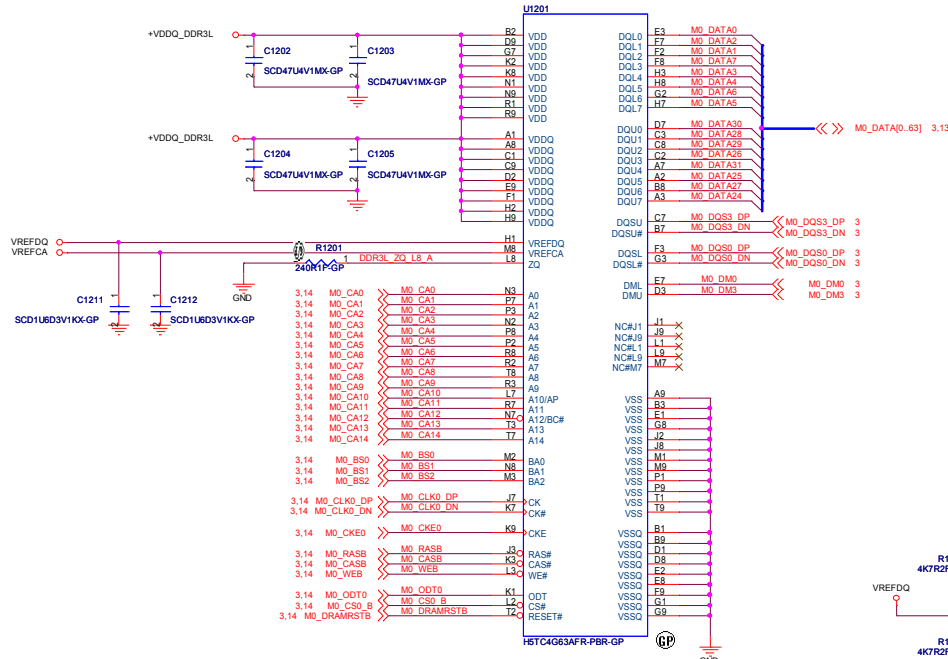
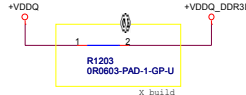
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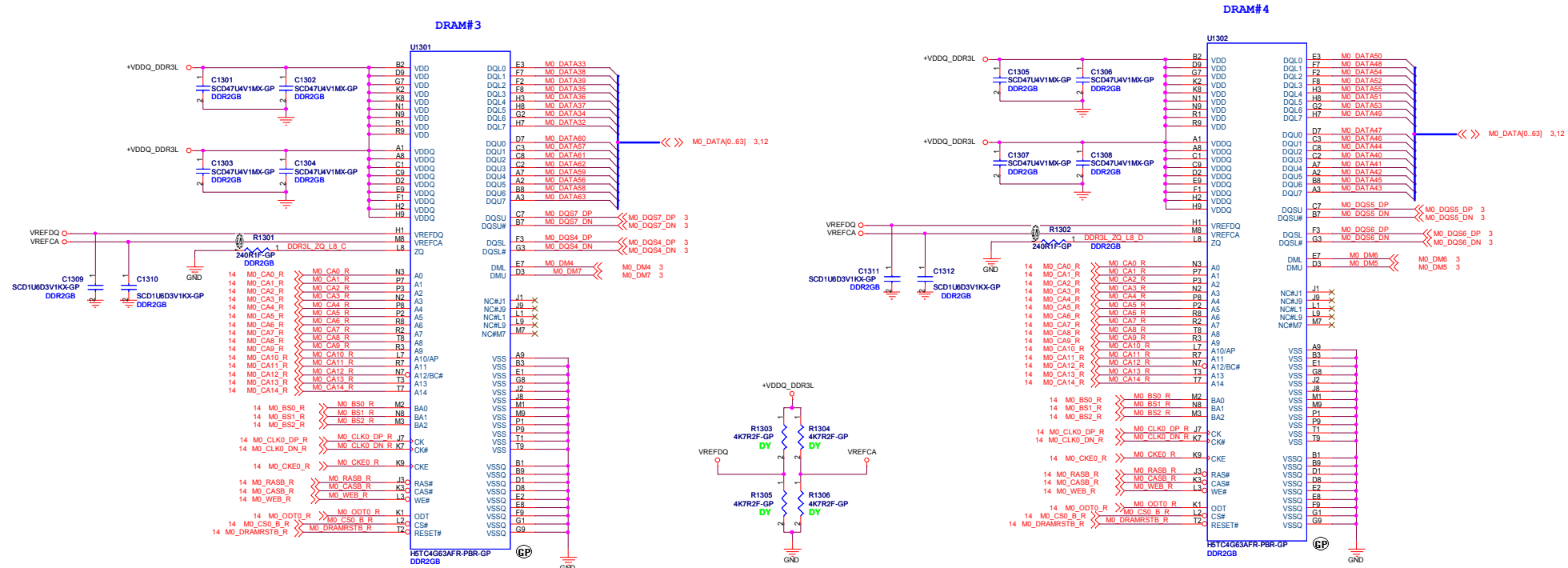
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## DDR3L SDRAM (CHANNEL0-1)



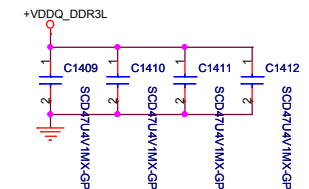
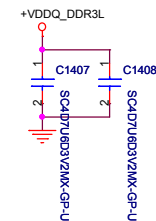
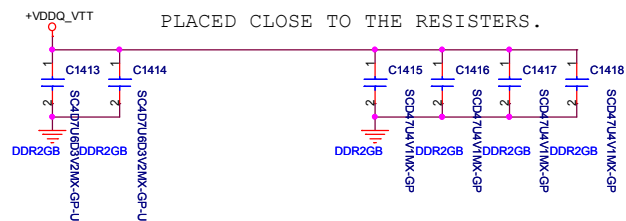
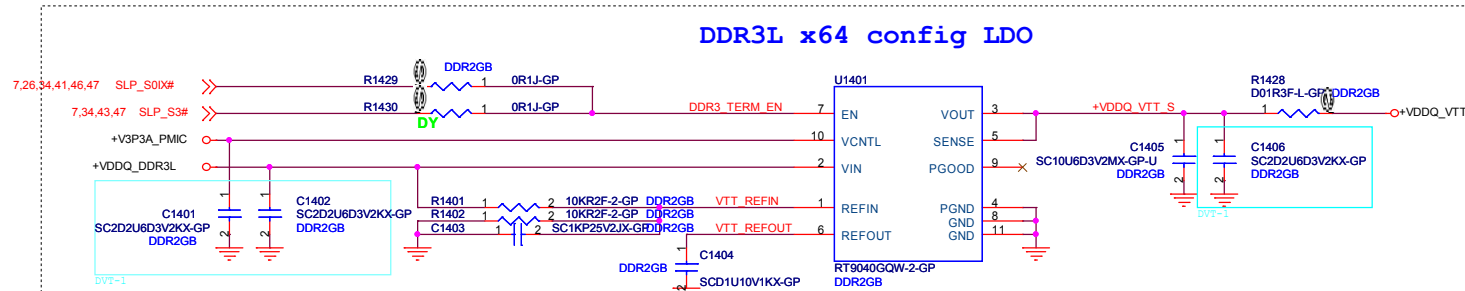
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# DDR3L SDRAM (CHANNEL0-2)



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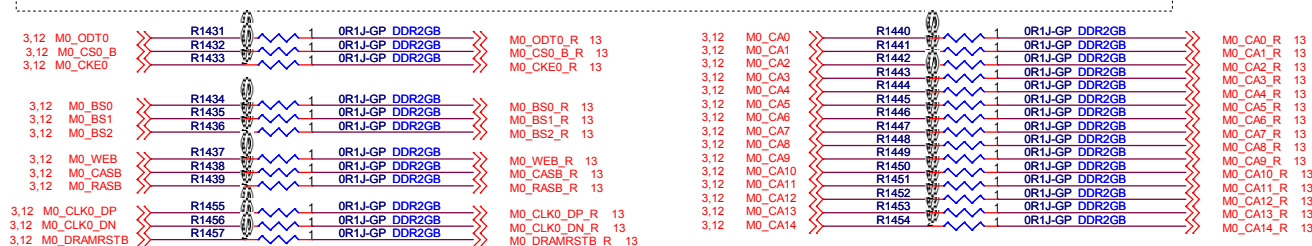
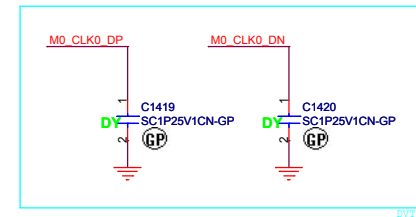
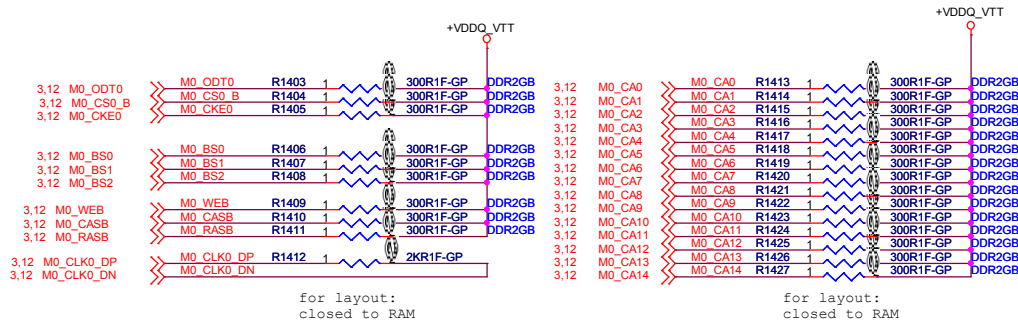
## DDR3L TERMINATIONS



### PLACED BETWEEN DRAM DEVICES

## STITCHING CAPS ON +VDDQ RAIL

## DDR3L TERMINATION



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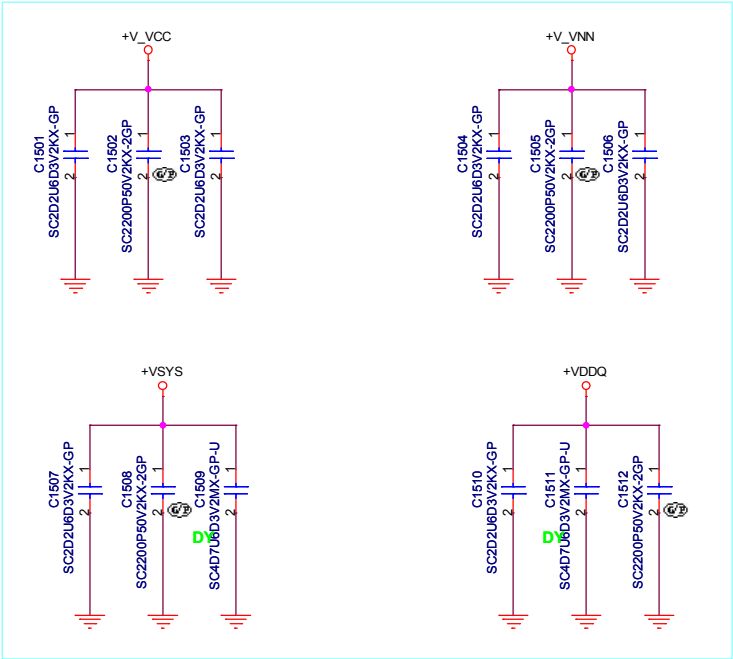
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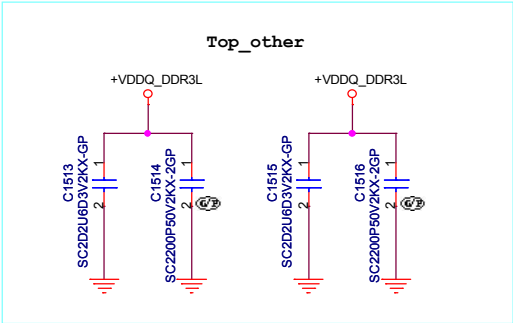
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RF\_Reserd CAP

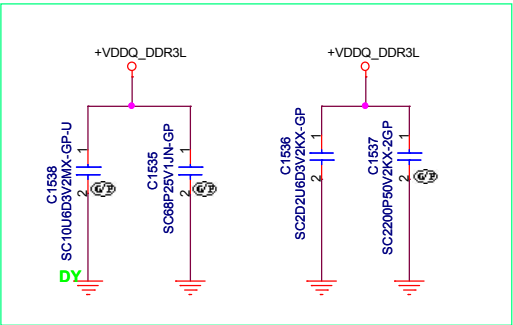
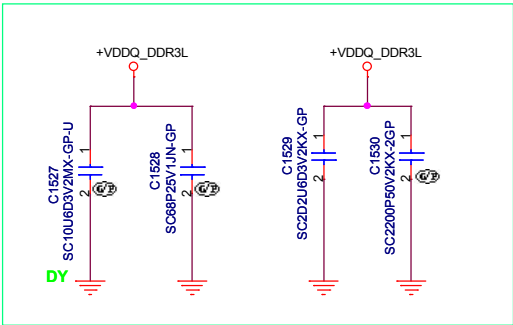
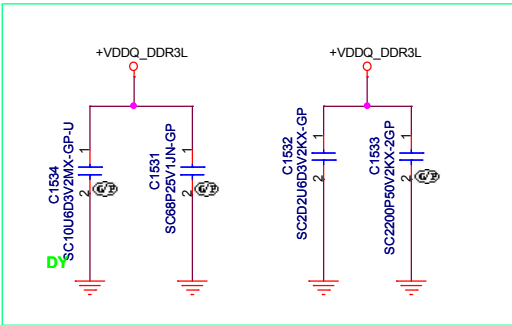
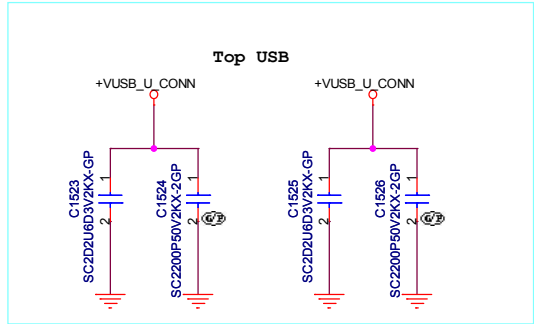
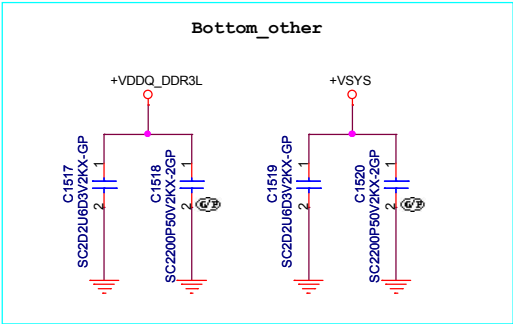
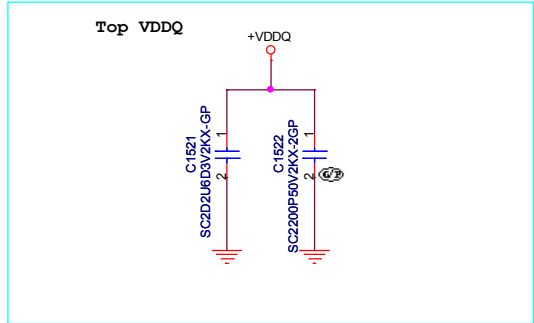
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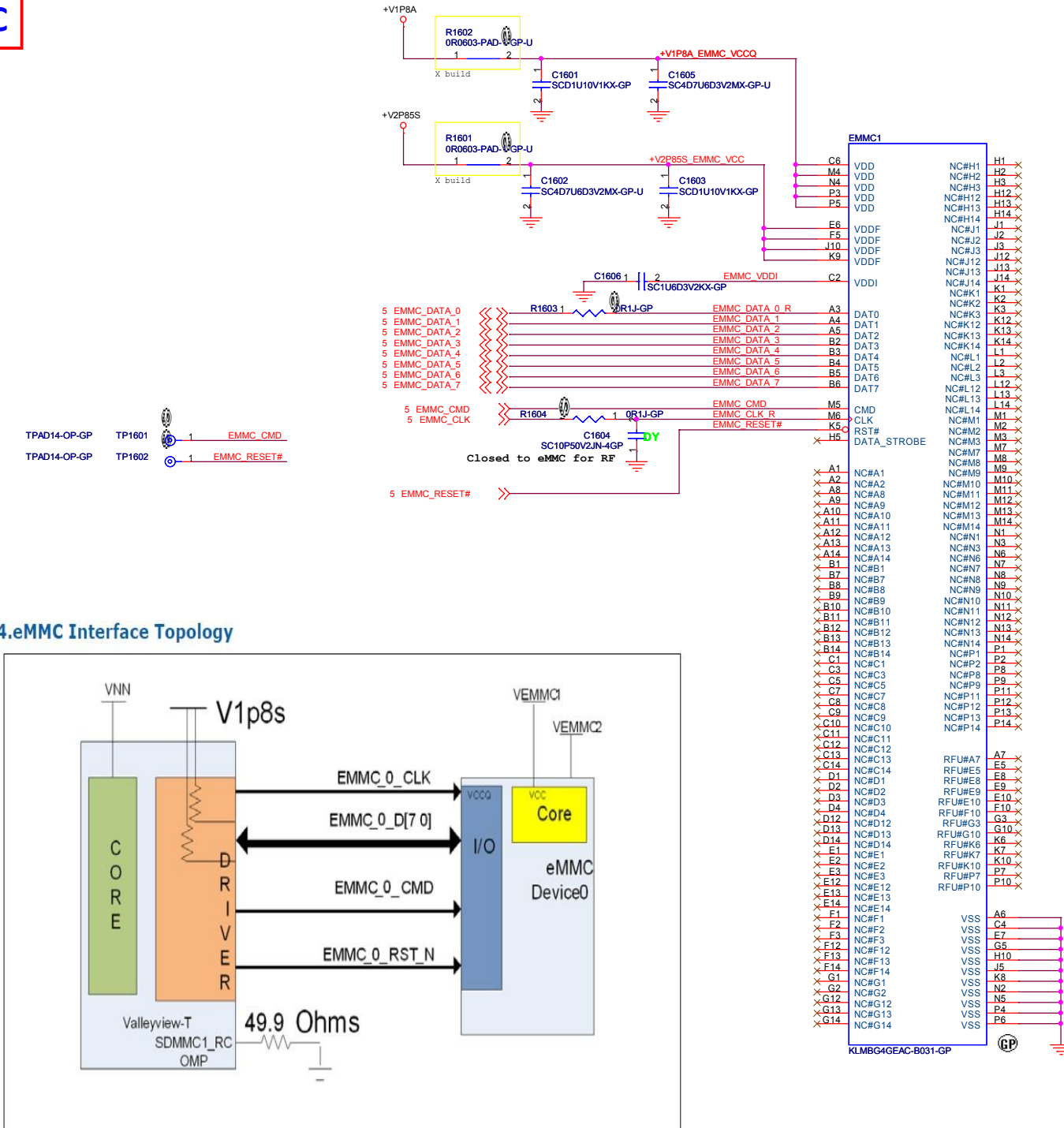


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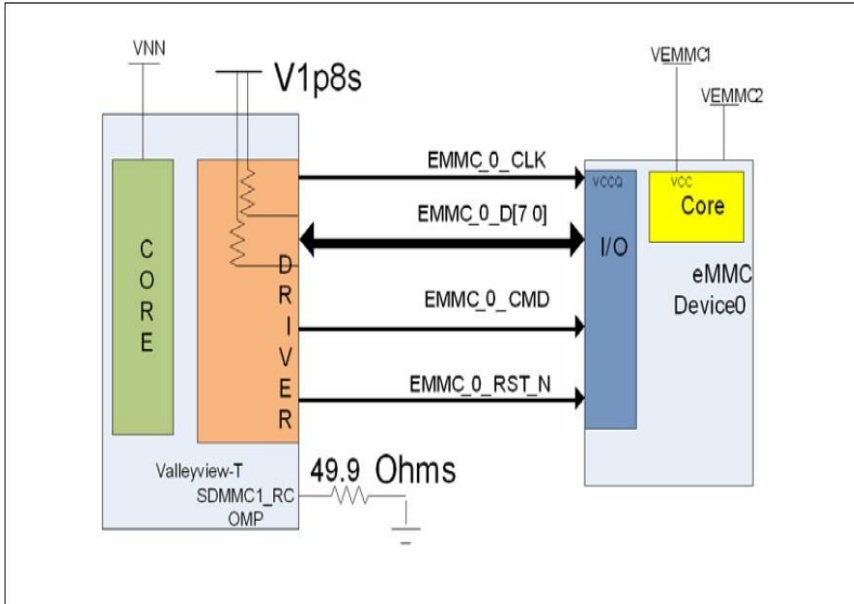


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**eMMC**



### Figure 3-44.eMMC Interface Topology



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**<Variant Name>**

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## 16 eMMC

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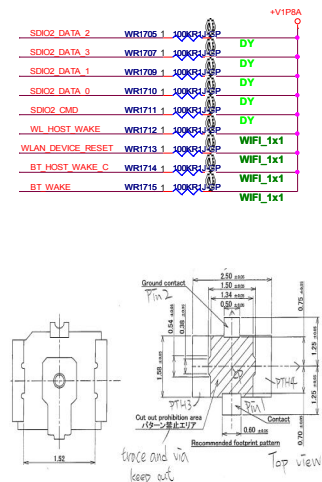
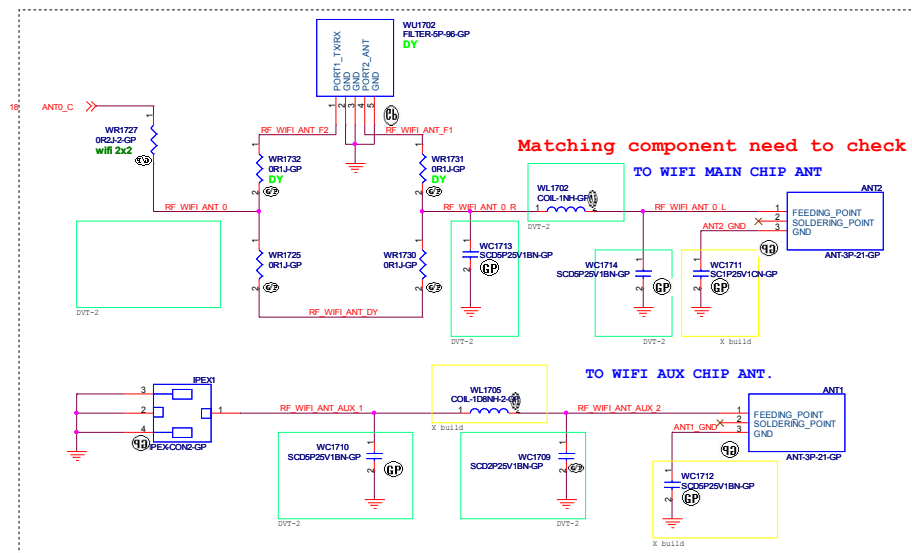
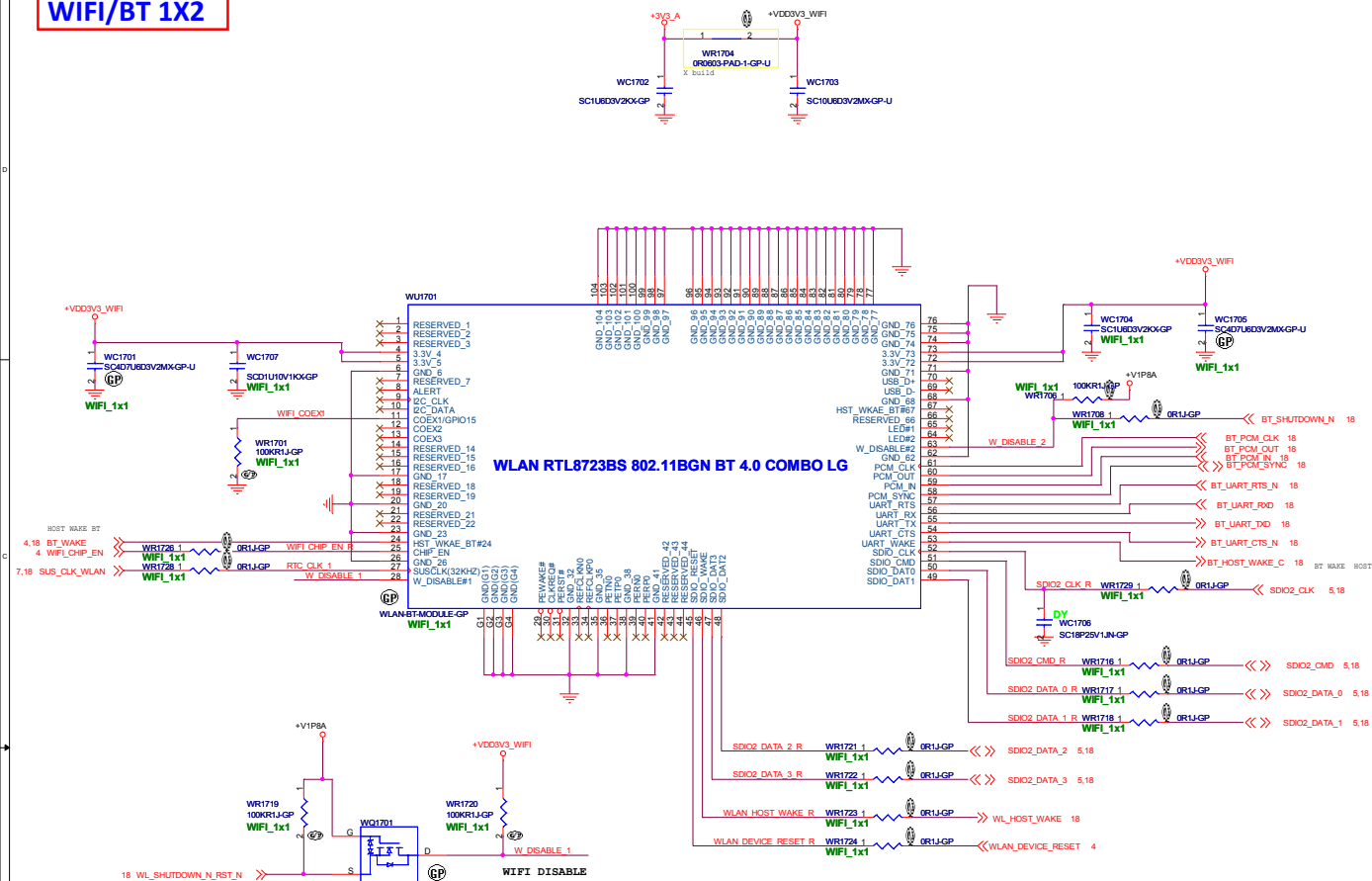
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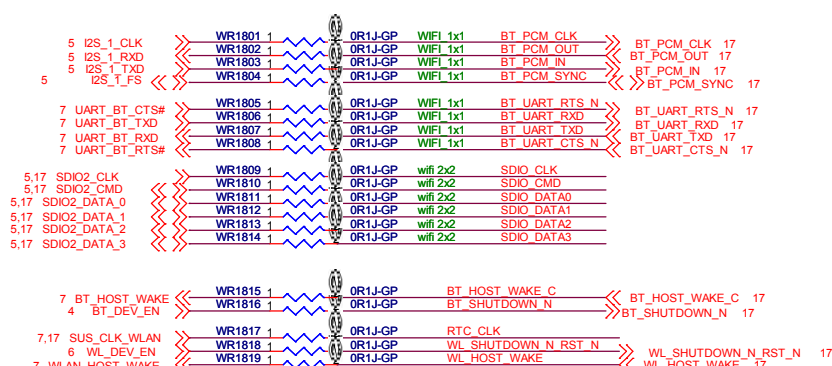
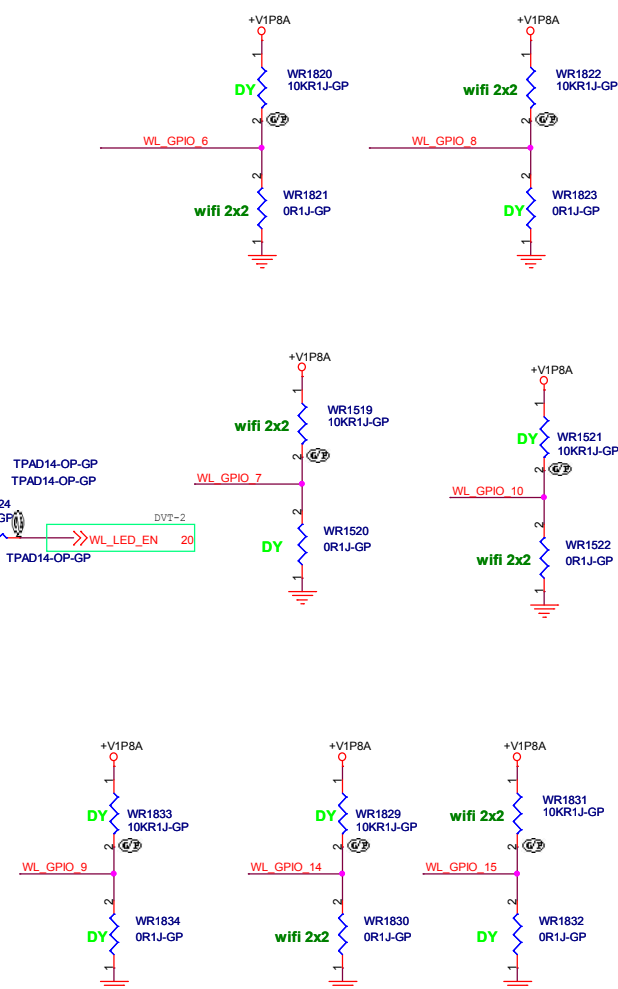
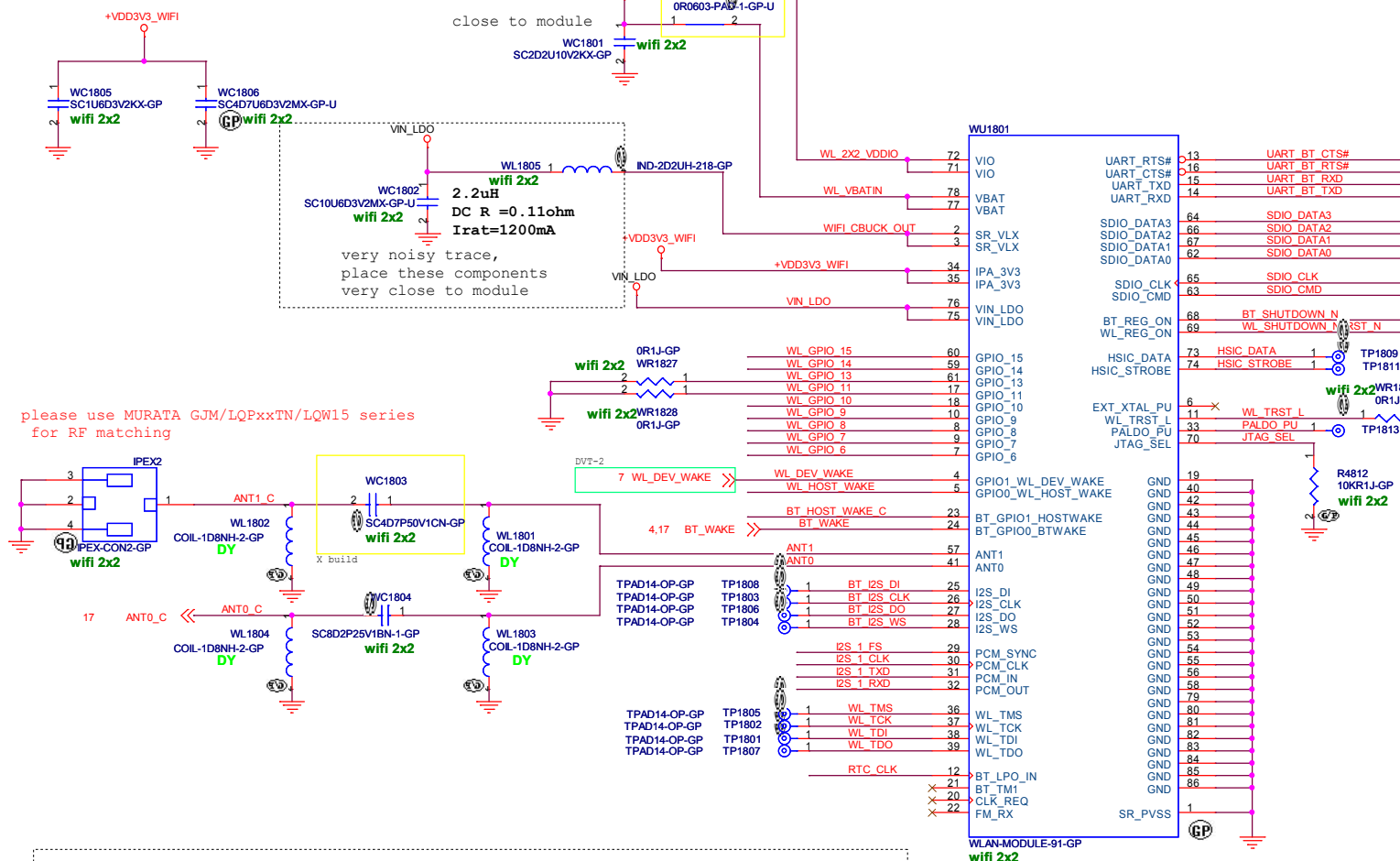


**WIFI/BT 1X2**



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**WIFI/BT 2X2 USI**



Mode	VIO	GPIO_6	GPIO_8	GPIO_7	GPIO_10	GPIO_14	GPIO_1
HSIC	3.3V	Pu	Pd	Pu	Pd	Pd	Pu
SDIO3.0	1.8V	Pd	Pu				
SDIO2.0	1.8V	Pd	Pu				
SDIO2.0	3.3V	Pd	Pd				

\*\* Pu : 4.7kohm Pulled up to VIO  
\*\* Pd : 0ohm Pulled down to GND

Mode	GPIO[6]	SDIO DATA2	SDIO DATA3
SDIO	0	X	X
gSPI	1	0	X
Normal HSIC	1	1	0
Bootloaderless HSIC	1	1	1

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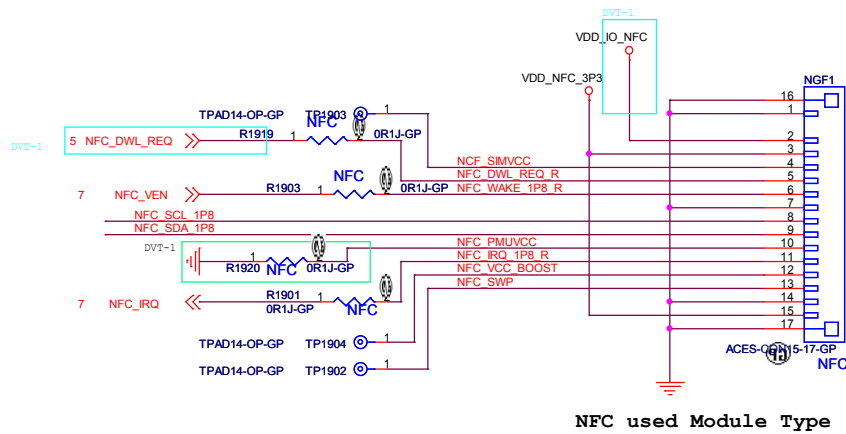
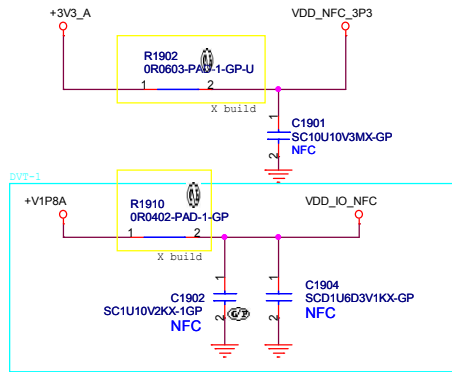
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Title **18 WIF/RT**

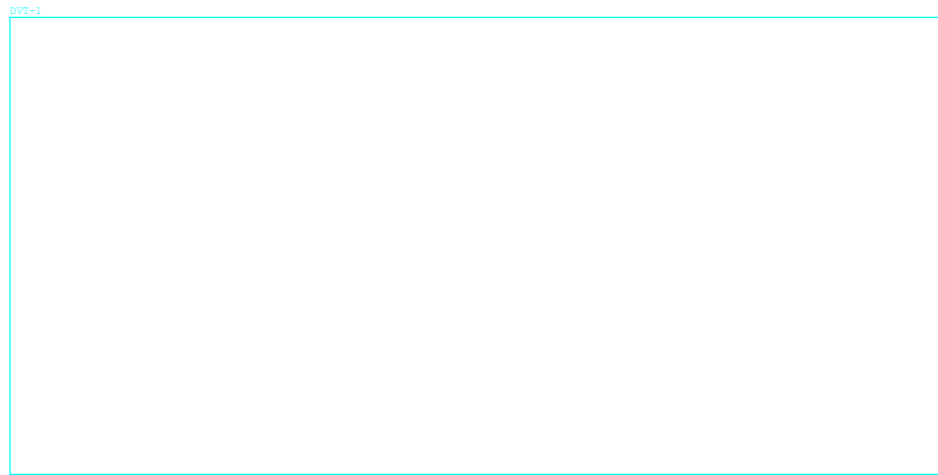
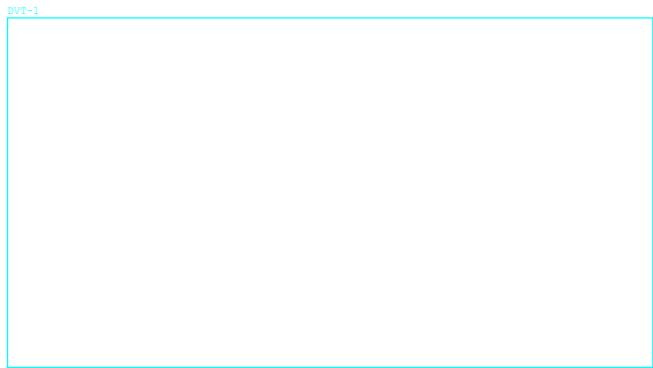
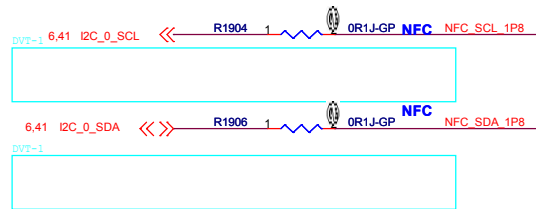
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NFC



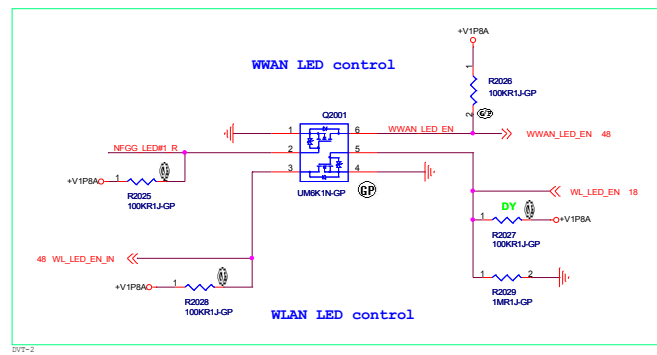
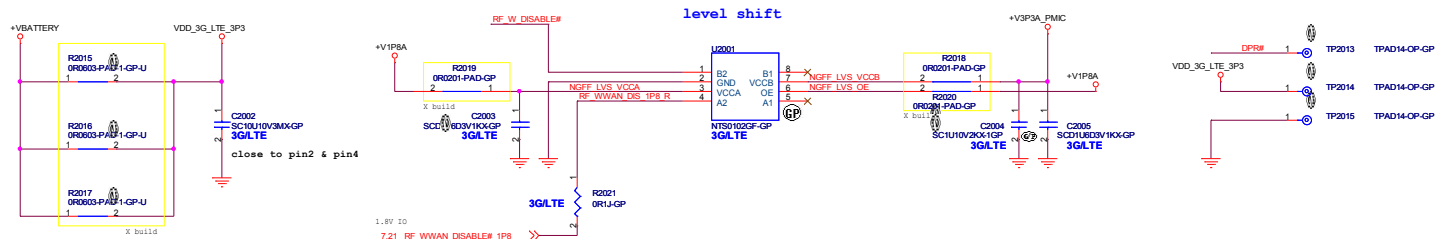
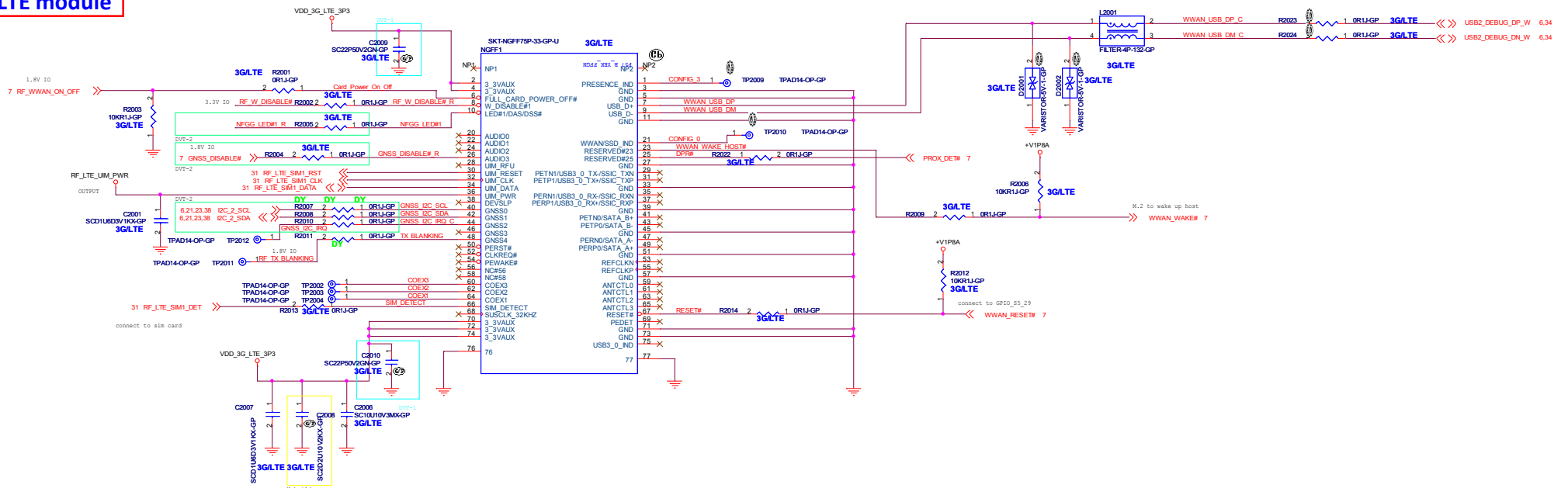
Pin number	Name
1	MOD_VDD
2	MOD_GND
3	SWP
4	VCC_BOOST
5	IRQ
6	PMUVCC
7	I <sup>2</sup> C_SDA
8	I <sup>2</sup> C_SCL
9	MOD_GND
10	Reset/Wakeup
11	DWL_REQ
12	SIMVCC
13	MOD_VDD
14	VDD_IO
15	MOD_GND



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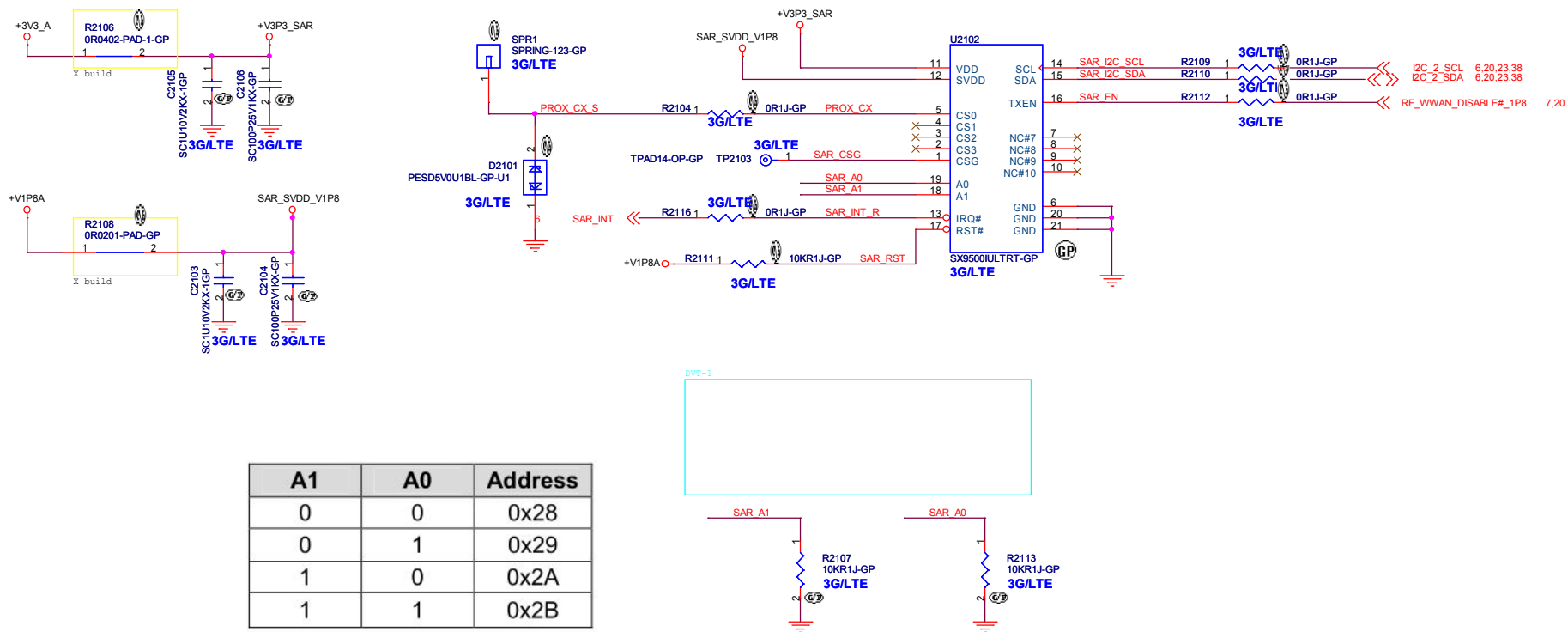
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### 3G/LTE module



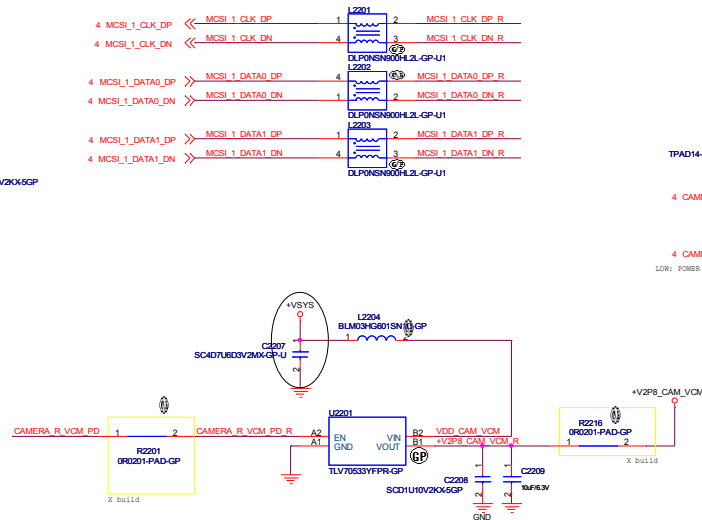
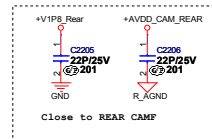
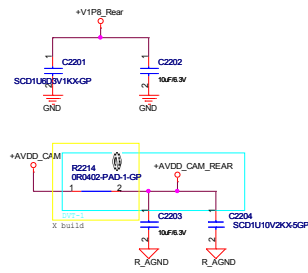
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# SAR sensor for 3G/LTE



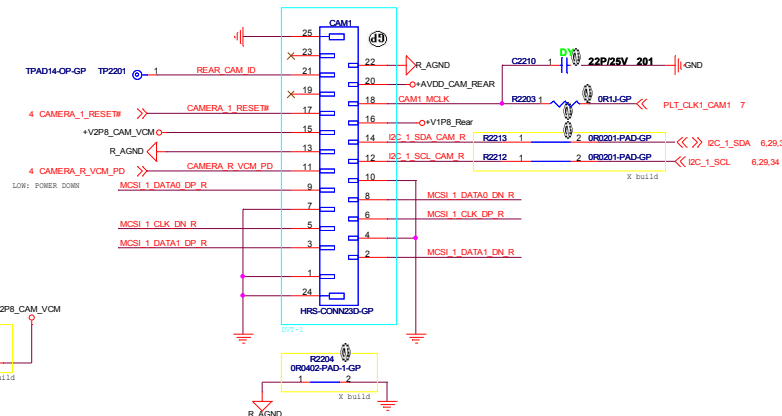
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## Rear Camera

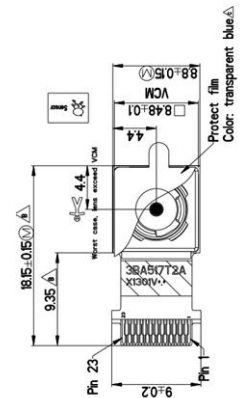
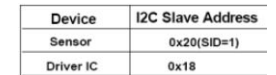


**Rear Camera**  
**OV5693(5M)**  
**13P2BA520(5M)**

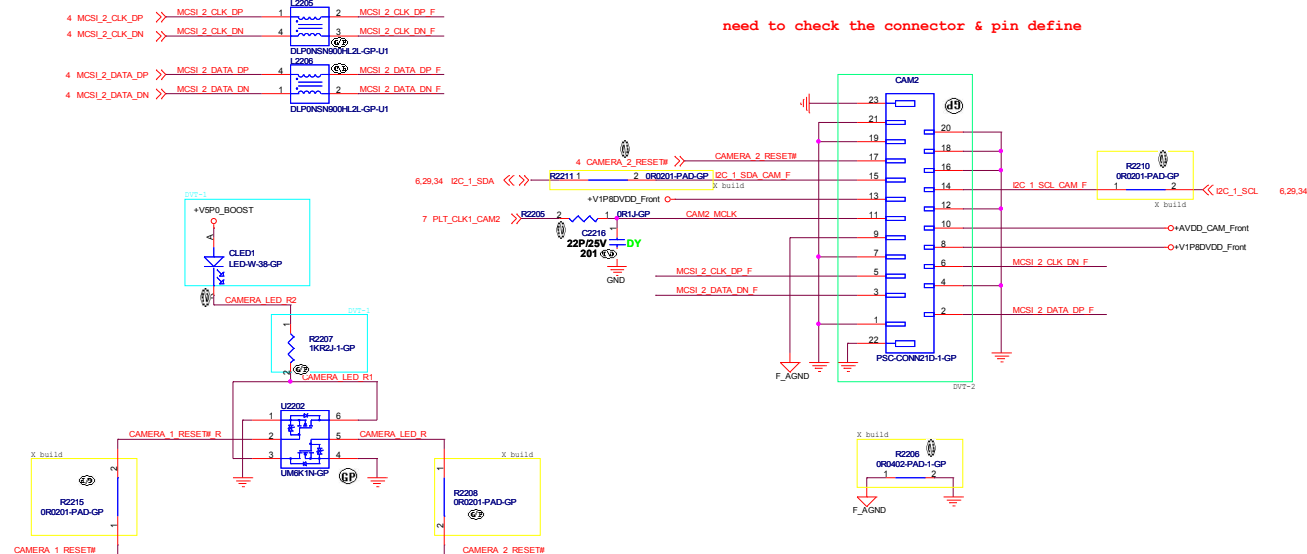
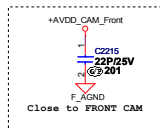
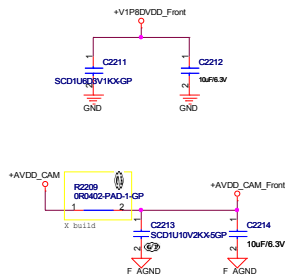
need to check the connector & pin define



CN Table	
No.	Signal
1	DGND
2	Data_N.2
3	Data_P.2
4	DGND
5	CLK_N
6	CLK_P
7	DGND
8	Data_N.1
9	Data_P.1
10	DGND
11	VCIN_PD
12	SCLK
13	AGND
14	SDATA
15	VCIN_VDD
16	VDD
17	CAM_PD
18	MCLK
19	NC
20	AVDD
21	Flash(ID)
22	AGND
23	NC



## Front Camera



Front Camera  
SOC1040(1.2M)  
13P2SF130(1.2M)

need to check the connector & pin define

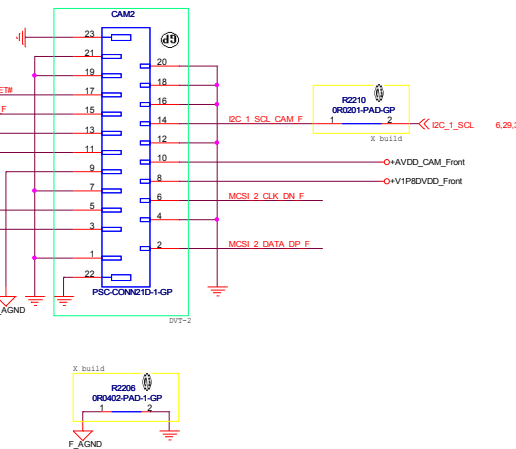

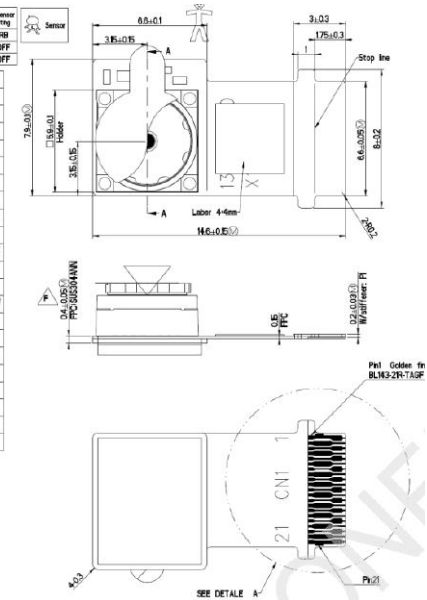


Image Orientation for location and pin are as follows

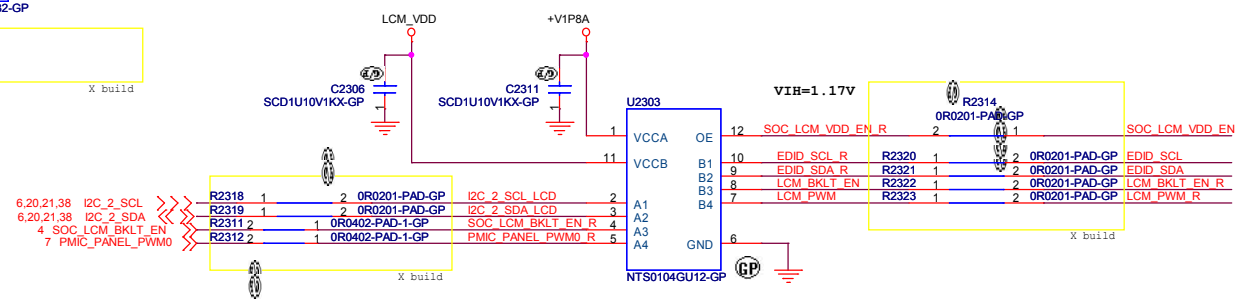
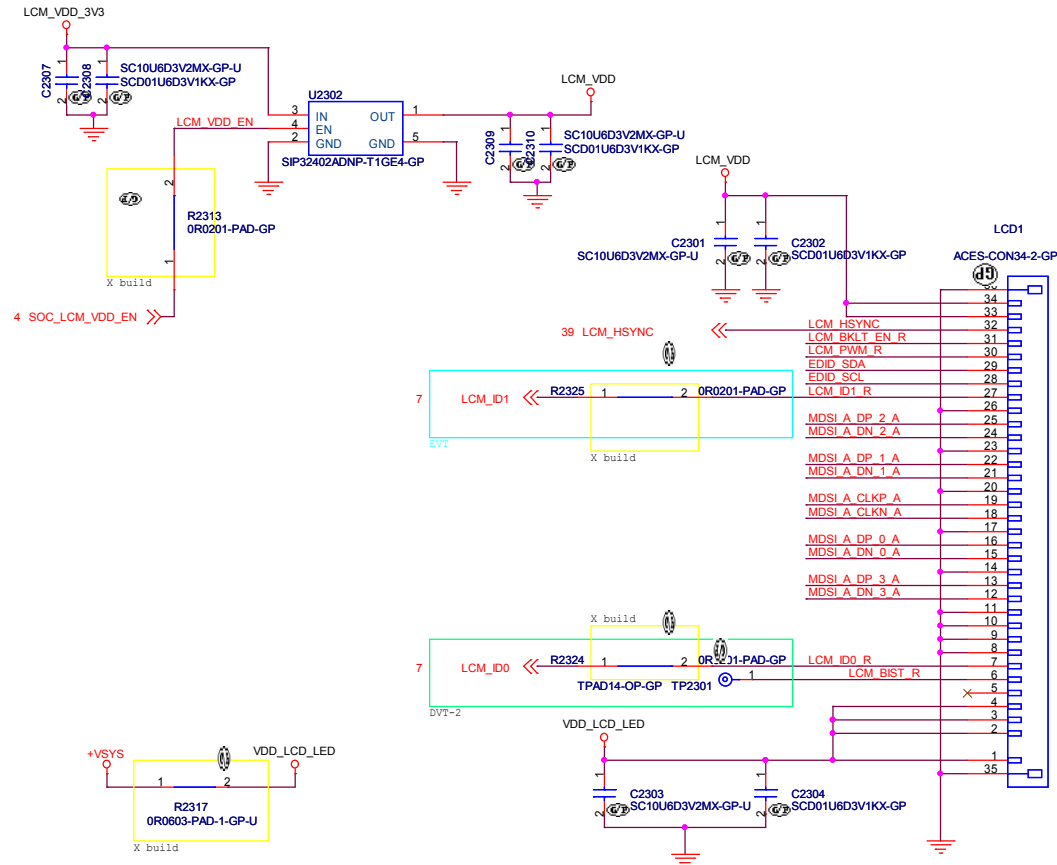
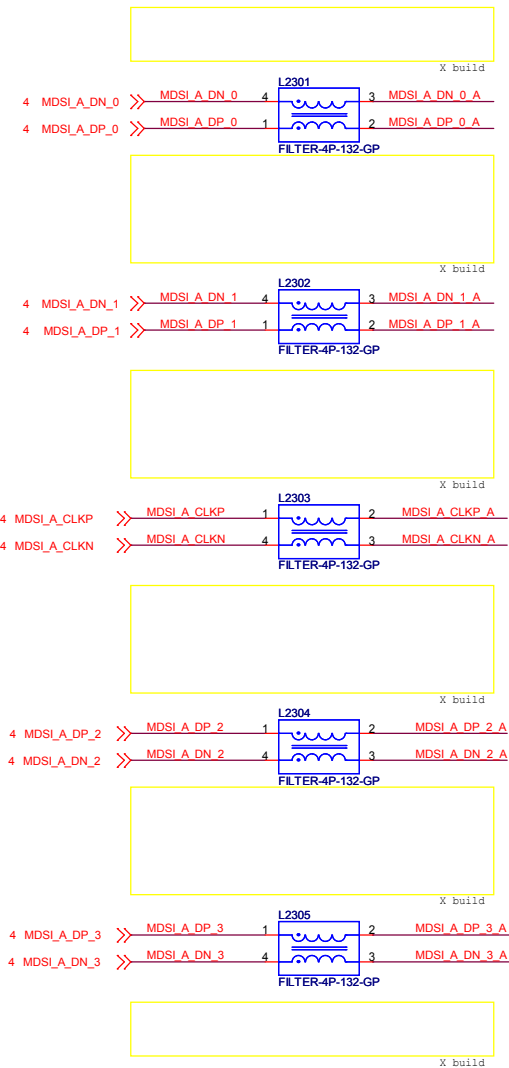
	Pin
	Y H

Connector CN	
1	DGND
2	DATA_P
3	DATA_N
4	DGND
5	CLK_P
6	CLK_N
7	DGND
8	DVDD 1.8V
9	AGND
10	AVDD 2.5V
11	MCLK
12	DGND
13	DVDD 1.8V
14	SI0C
15	SI0D
16	DGND
17	RESET
18	DGND
19	0ND
20	0ND
21	0ND



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**MIPI LCM 19x12**



Each port I/O has an internal  
10 k  $\Omega$  pull-up resistor to VCC(A)/VCC(B)

No.	Pin Name	Pin Name Description
1	VDD	DC-DC circuit supply voltage (3V~3.8V)
2	VDD	DC-DC circuit supply voltage (3V~3.8V)
3	H <sub>sync</sub>	H <sub>sync</sub>
4	LED_EN	LED driver Enable Input (VIH=1.8V)
5	LED_PWM	Backlight LED driver PWM Input (VIH=1.8V)
6	EDID_SDA	EDID Data Input (VIH=1.8V)
7	EDID_SCL	EDID Clock Input (VIH=1.8V)
8	ID	NC
9	GND	Ground
10	DSI_D2P/Rx-IN2P	MIPI data pair 2 positive signal
11	DSI_D2N/Rx-IN2N	MIPI data pair 2 negative signal
12	GND	Ground
13	DSI_D1P/Rx-IN1P	MIPI data pair 1 positive signal
14	DSI_D1N/Rx-IN1N	MIPI data pair 1 negative signal
15	GND	Ground
16	DSI_CLKP/Rx-CLKP	MIPI Clock positive signal
17	DSI_CLKN/Rx-CLKN	MIPI Clock negative signal
18	GND	Ground
19	DSI_D0P/Rx-IN0P	MIPI data pair 0 positive signal
20	DSI_D0N/Rx-IN0N	MIPI data pair 0 negative signal
21	GND	Ground
22	DSI_D3P/Rx-IN3P	MIPI data pair 3 positive signal
23	DSI_D3N/Rx-IN3N	MIPI data pair 3 negative signal
24	GND	Ground
25	GND	Ground
26	GND	Ground
27	GND	Ground
28	ID	Ground
29	BIST	Aging Mode Power Supply
30	NC	Not Connection
31	LED+	LED Power Supply (3V ~ 5V)
32	LED+	LED Power Supply (3V ~ 5V)
33	LED+	LED Power Supply (3V ~ 5V)
34	LED+	LED Power Supply (3V ~ 5V)

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Title	<b>23_MIPI LCM CONN</b>
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MIPI LCM 19x8

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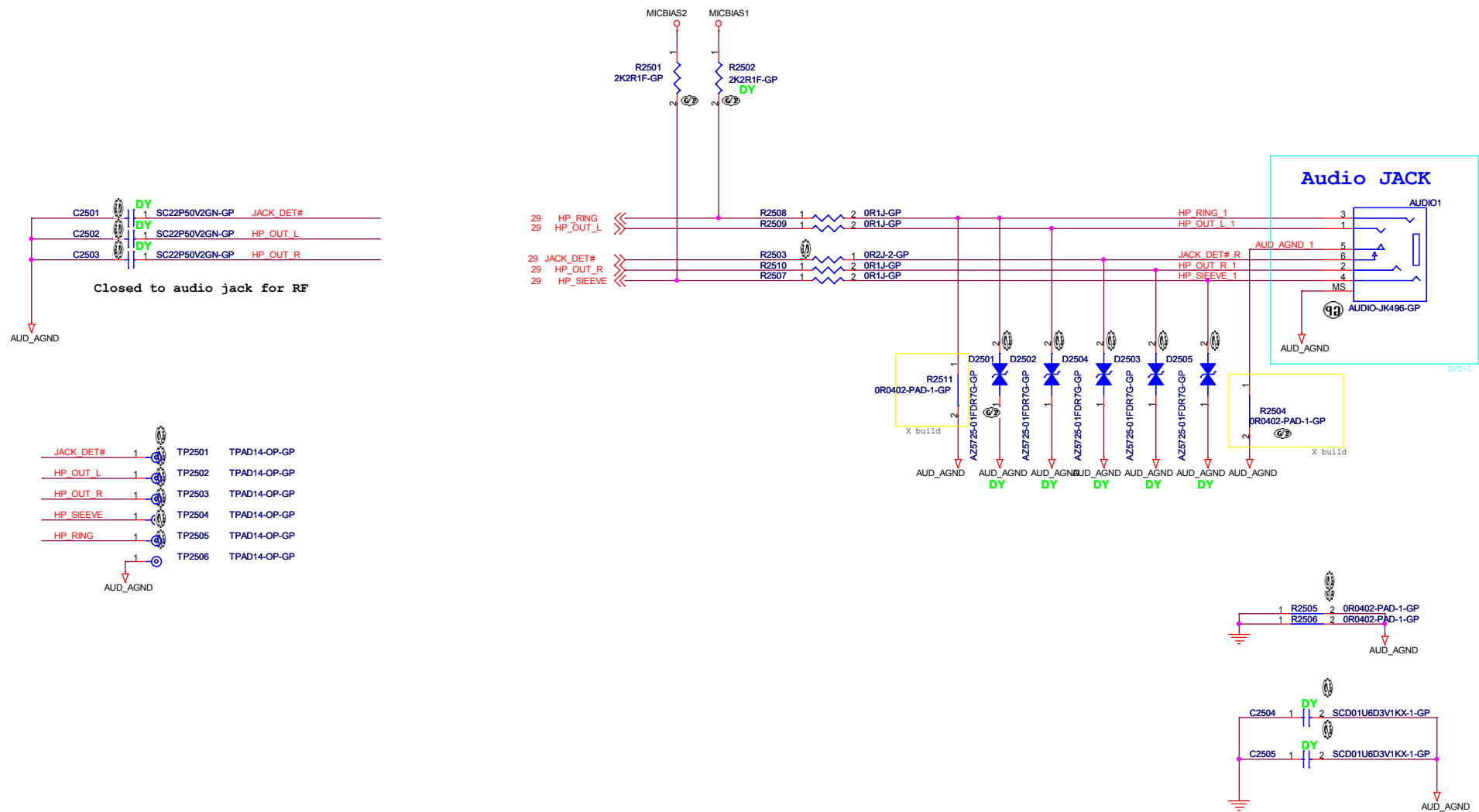
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Title			24_MIPI LCM CONN		
Size	Document Number				Rev
A	SILVERTON/SILVEROAK				0
Date:	Saturday, July 19, 2014			Sheet 24 of	61



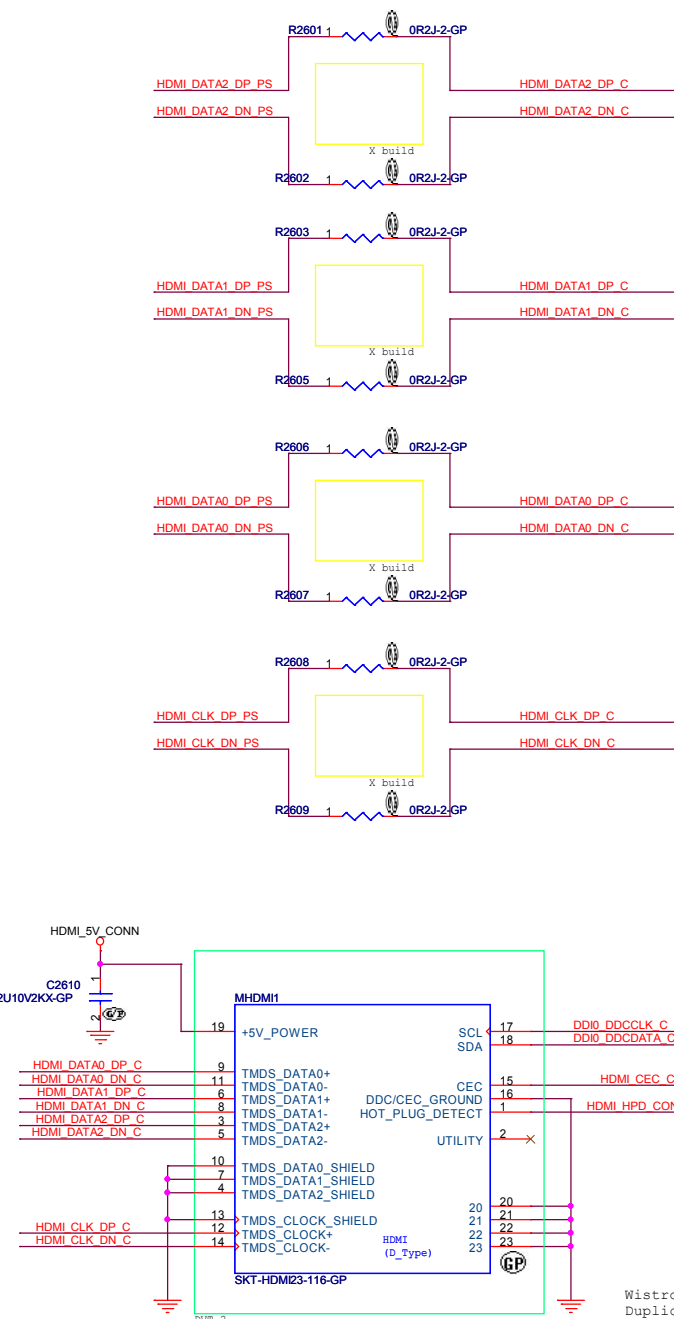
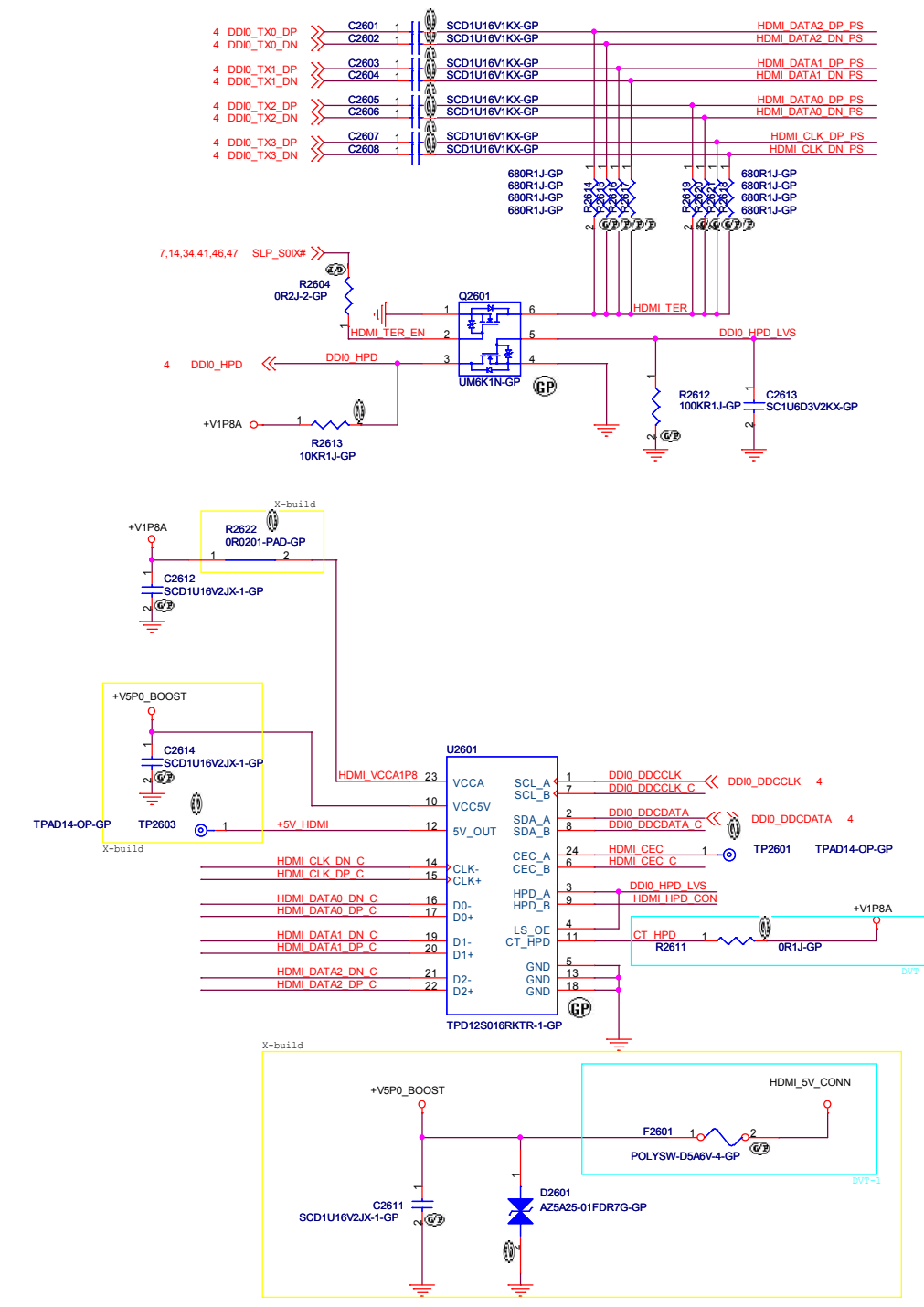
# Device :AUDIO JACK



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Title 25_Audio JACK			
Size A3	Document Number SILVERTON/SILVEROAK		Rev 0
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# Device :uHDMI



Pin	Pin定義
1	Hot Plug Detect
2	Utility
3	TMDS Data2+
4	TMDS Data2 Shield
5	TMDS Data2-
6	TMDS Data1+
7	TMDS Data1 Shield
8	TMDS Data1-
9	TMDS Data0+
10	TMDS Data0 Shield
11	TMDS Data0-
12	TMDS Clock+
13	TMDS Clock Shield
14	TMDS Clock-
15	CEC
16	DDC/CEC Ground
17	SCL
18	SDA
19	+5V Power

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Title26\_uHDMI CONN

SizeA3Document NumberSILVERTON/SILVEROAKRev0

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Title			27_Reserved		
Size	Document Number			Rev	
A	SILVERTON/SILVEROAK			0	
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Title			28_Reserved		
Size A	Document Number SILVERTON/SILVEROAK				Rev 0
Date:	Saturday, July 19, 2014		Sheet	28	of 61

# AUDIO CODEC

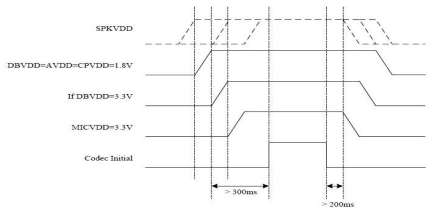
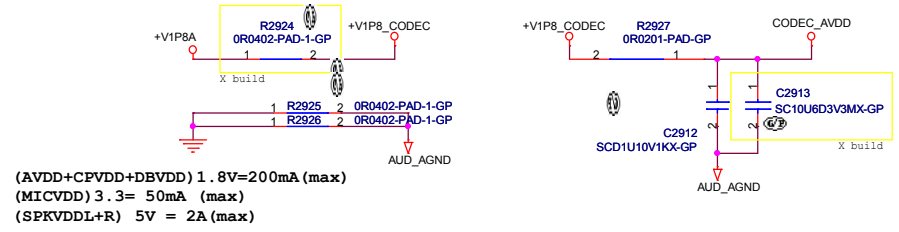
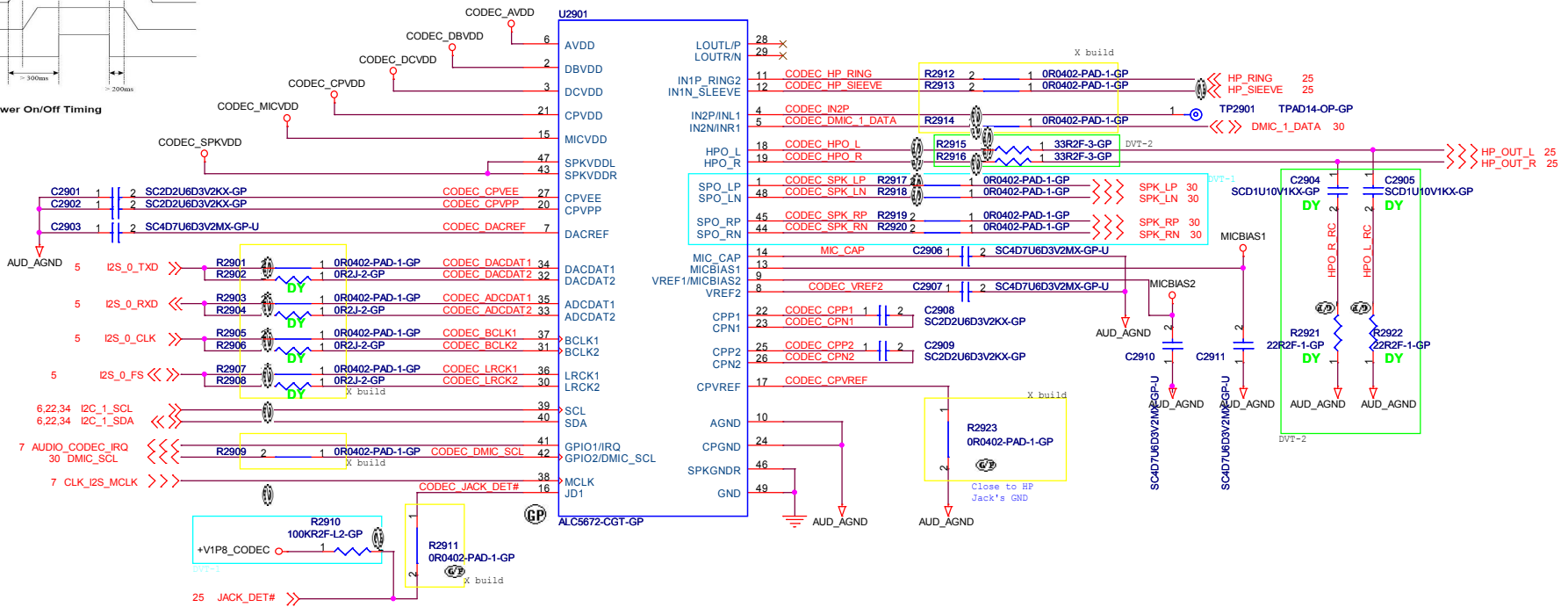
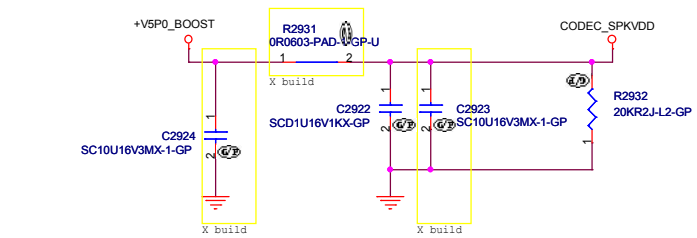
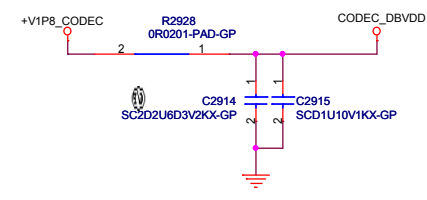
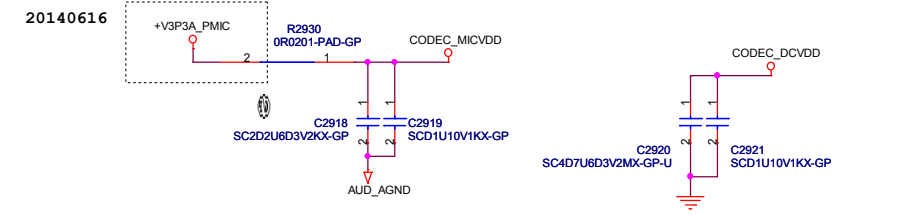


Figure 6. Power On/Off Timing



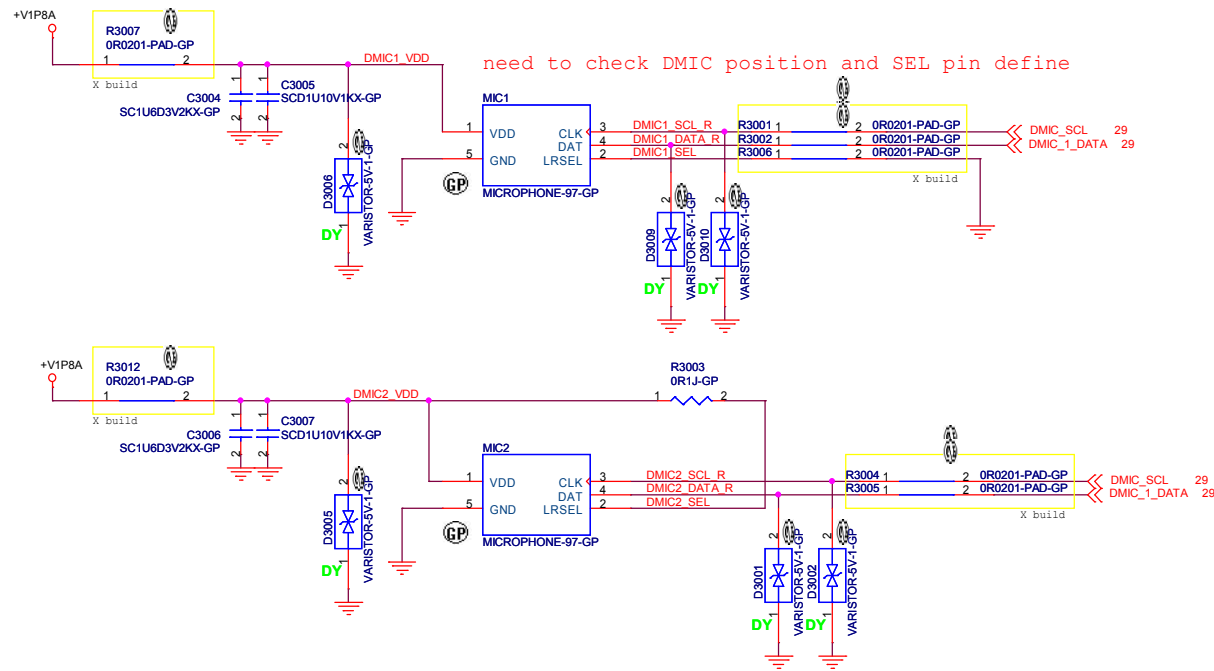
(AVDD+CPVDD+DBVDD) 1.8V=200mA (max)  
(MICVDD) 3.3= 50mA (max)  
(SPKVDDL+R) 5V = 2A(max)



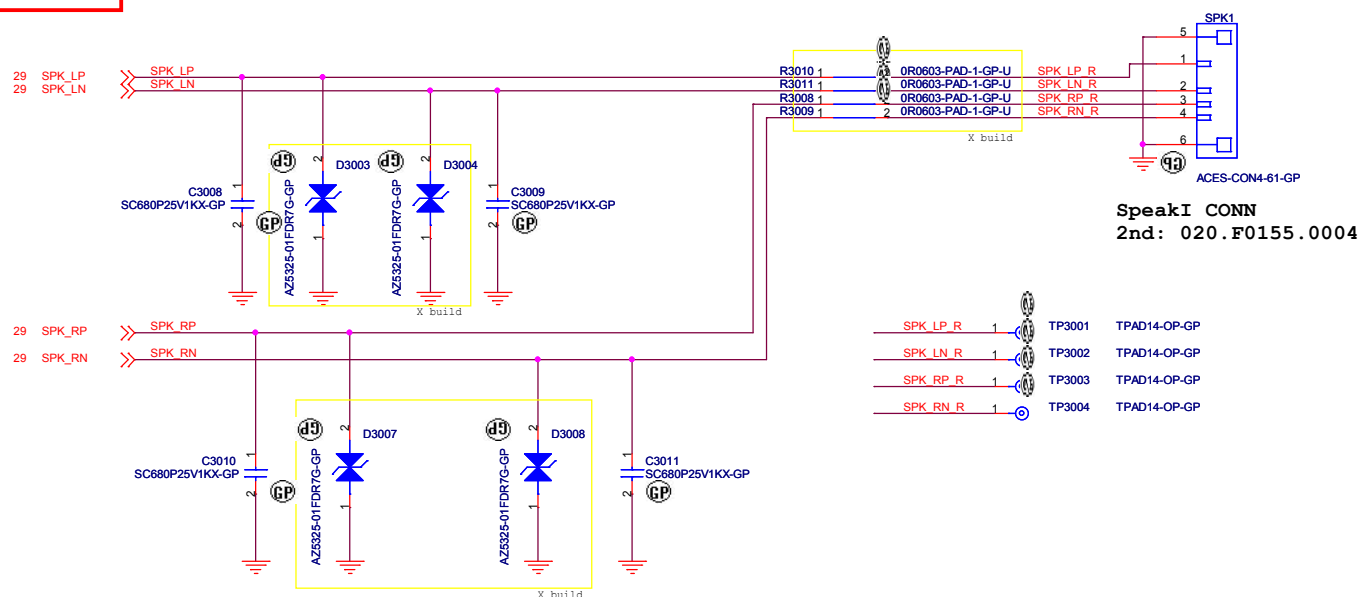
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Title	29_AUDIO CODEC
Size	A3
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# DMIC



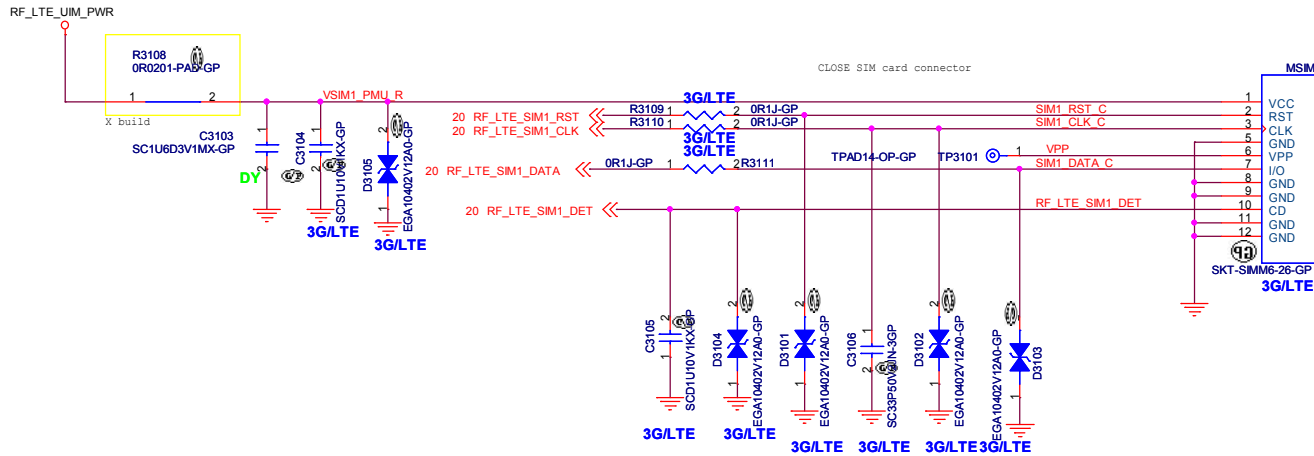
# SPEAKER



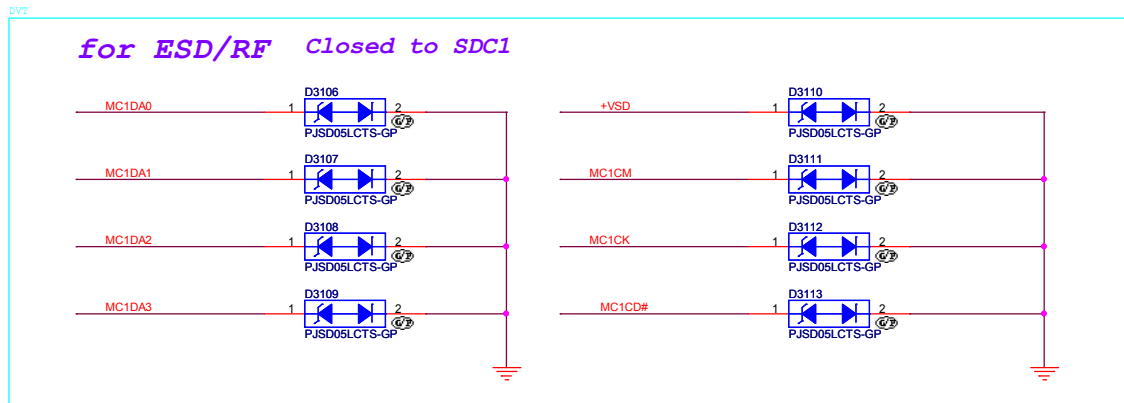
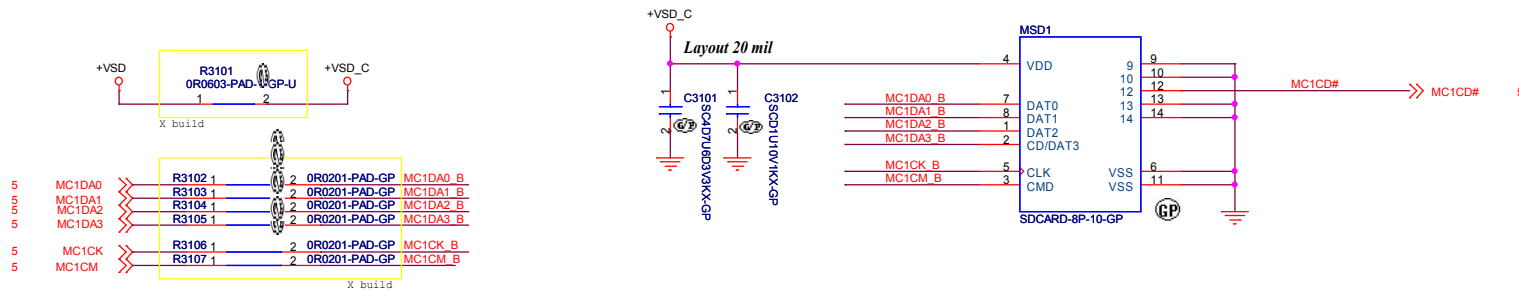
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Title	30_AUDIO DMIC/SPK
Size	Document Number
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# SIM CARD



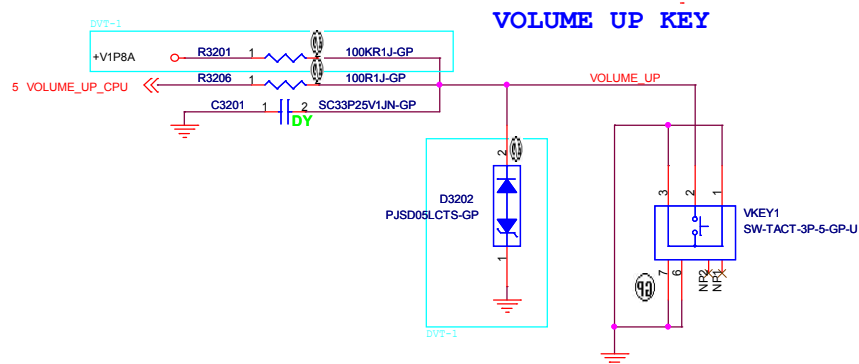
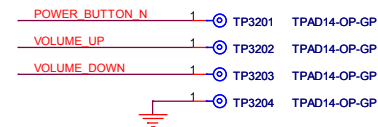
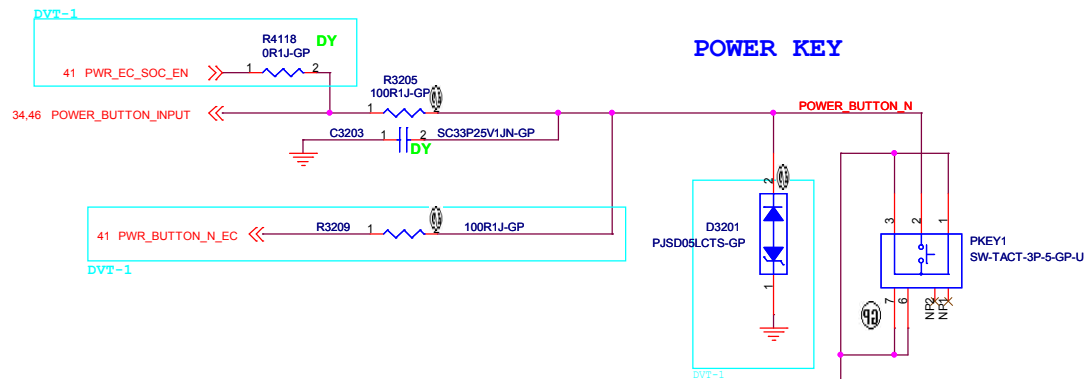
# SD CARD



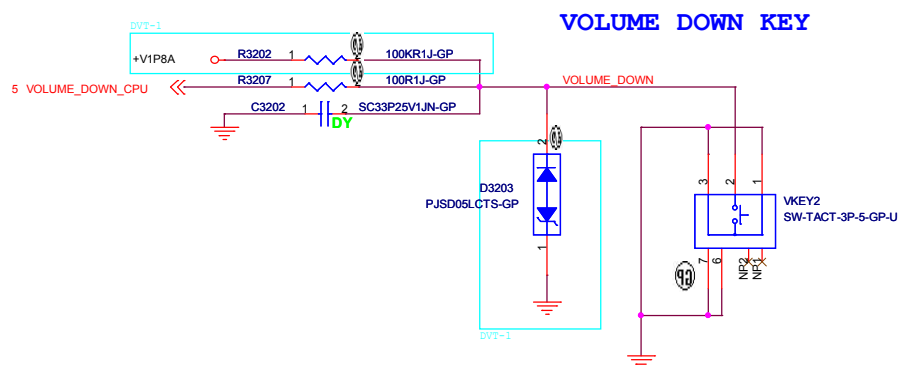
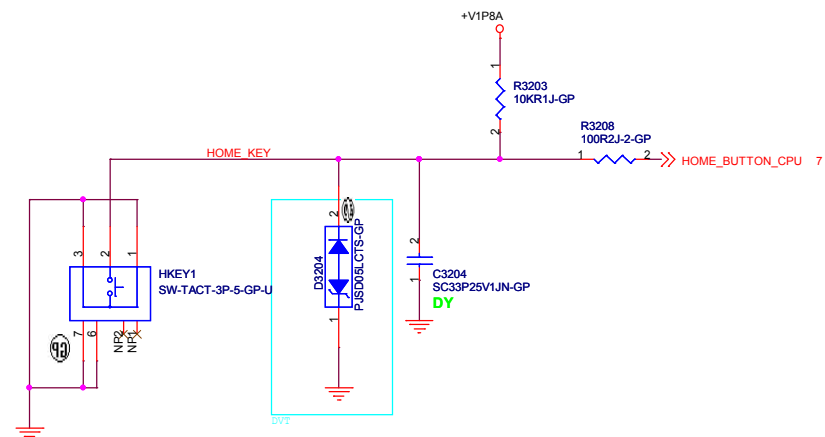
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Title			
<b>31_uSD/SIM Card CONN</b>			
Size A3	Document Number <b>SILVERTON/SILVEROAK</b>		Rev <b>0</b>
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# PWR Button / Volum Key / Home key



## HOME KEY



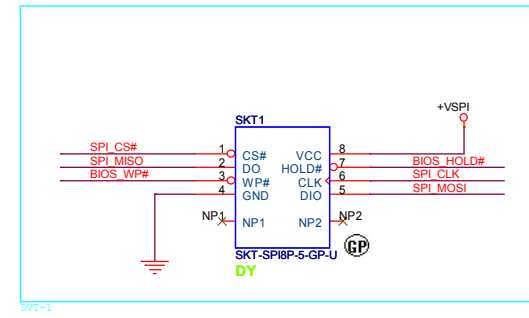
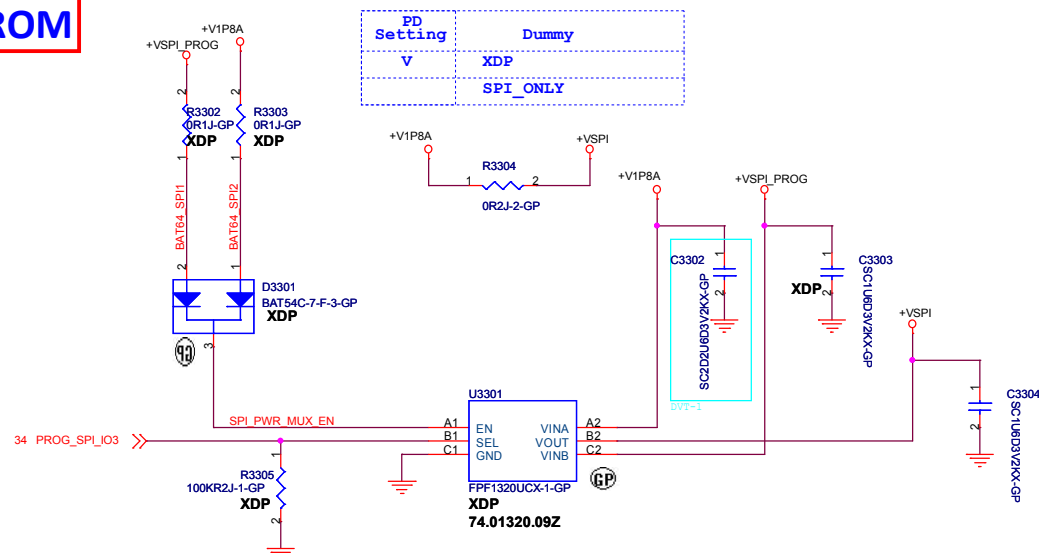
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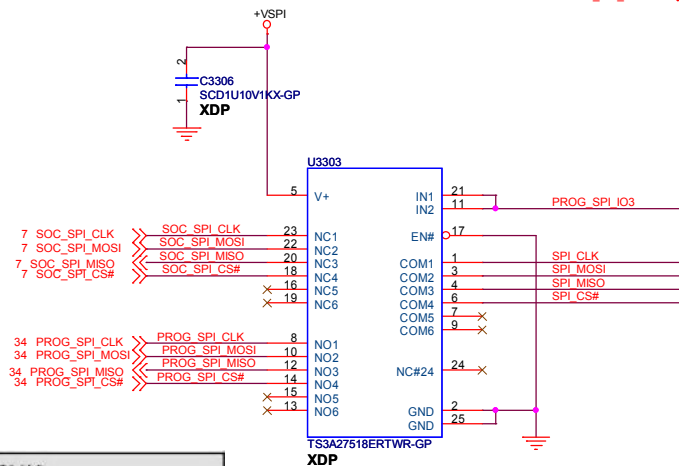
Title		32_PWR/Volume/Home Button
Size	Document Number	Rev
A3	SILVERTON/SILVEROAK	0
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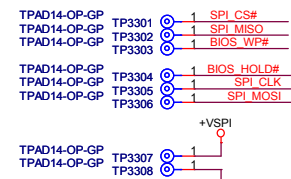
# SPI ROM



SPI POWER MUX DEFAULT --> LOW	
SEL = 0	+V1P8A from Platform
SEL = 1	+VSPI_PROG



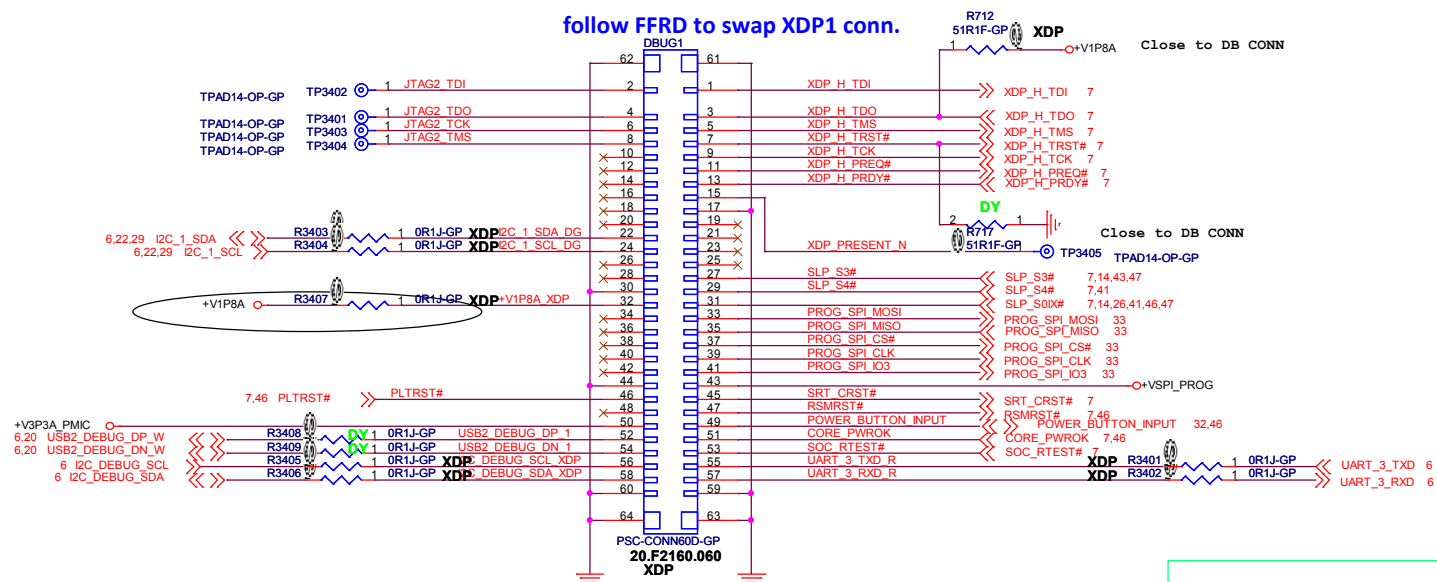
SPI MUX DEFAULT --> LOW	
IN1= IN2 = 0	SOC SPI Path
IN1= IN2 = 1	PROGRAMMING Path



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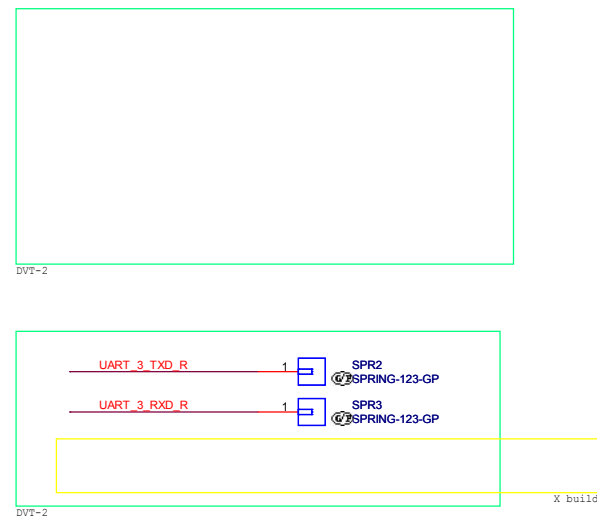
Title	
33_SPI NOR	
Size A3	Document Number SILVERTON/SILVEROAK
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Rev 0	

## XDP Debug Connector



## Debug Connector on board

N/C	2	1	XDP_TDI
N/C	4	3	XDP_TDO
N/C	6	5	XDP_TMS
N/C	8	7	XDP_TRST#
N/C	10	9	XDP_TCK
N/C	12	11	XDP_PREQ#
N/C	14	13	XDP_PRODY#
N/C	16	15	TP_XDP_PRESENT#
N/C	18	17	GND
N/C	20	19	N/C
SIO_I2C1_DATA	22	21	N/C
SIO_I2C1_CLK	24	23	N/C
N/C	26	25	N/C
N/C	28	27	PMC_SLP_S3#
GND	30	29	PMC_SLP_S4#
N/C	32	31	PMC_SLP_S0IX#
N/C	34	33	SPI_MOSI
N/C	36	35	SPI_MISO
N/C	38	37	SPI_CS#
N/C	40	39	SPI_CLK
N/C	42	41	PROG_SPI_IO3
GND	44	43	V1P8_SPI
PMC_PLTRST#	46	45	ILB_RTC_RST#
N/C	48	47	PMC_RSMRST#
N/C	50	49	PMC_PWRBTN#
USB2_DP	52	51	CORE_PWROK
USB2_DN	54	53	SOC_RTEST#
D1_I2C_CLK	56	55	UART3_TXD
D1_I2C_DATA	58	57	UART3_RXD
GND	60	59	GND



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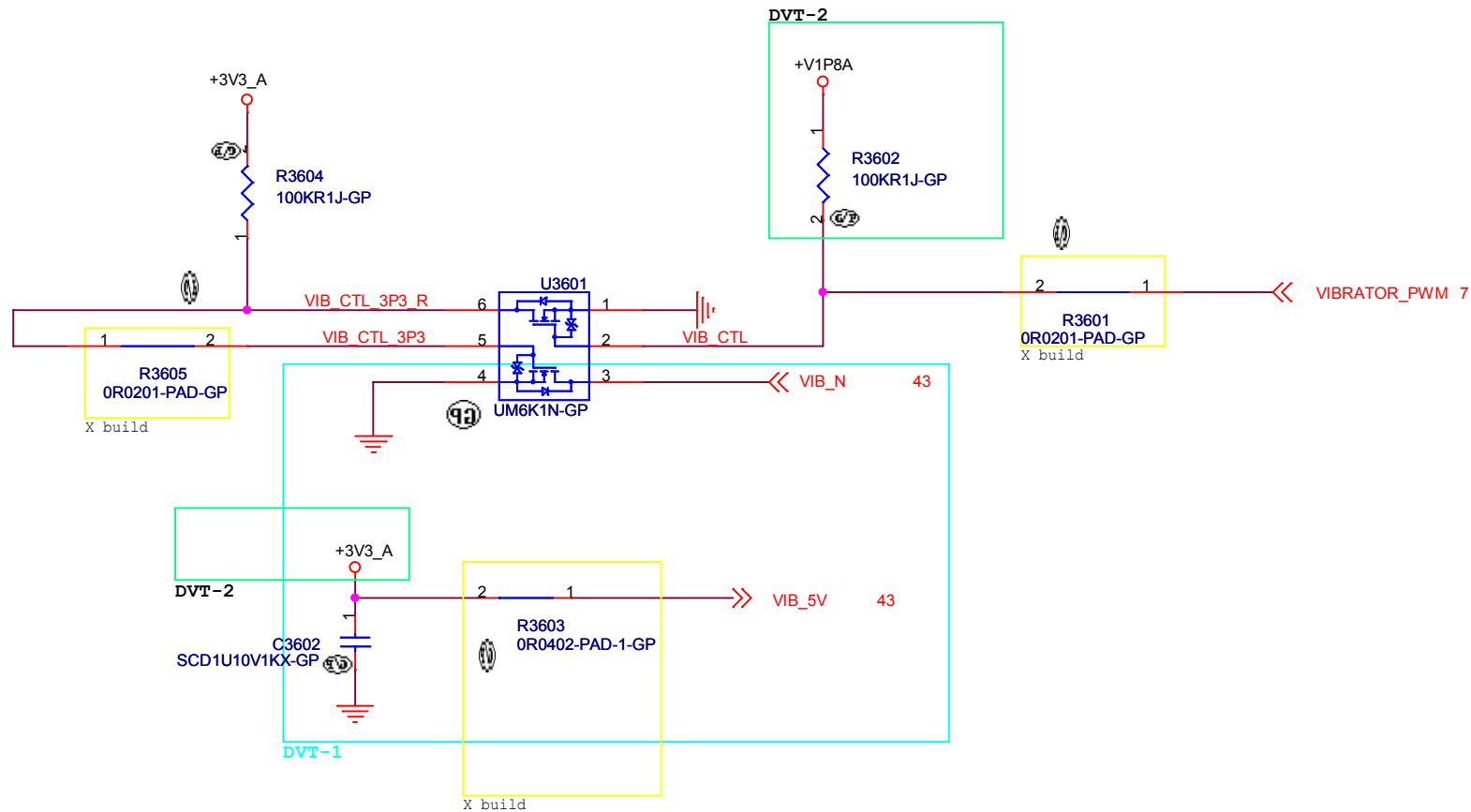
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Size A	Document Number SILVERTON/SILVEROAK				Rev 0
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## Vibrator



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Title	<b>36_Vibrator</b>
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Size A4	Document Number <b>SILVERTON/SILVEROAK</b>
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Rev	
C	

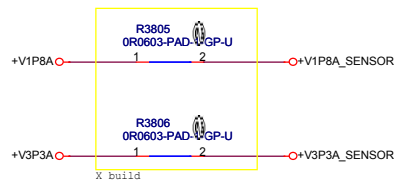
Date: Tuesday, December 09, 2014 Sheet 36 of 61

Thermal Protect

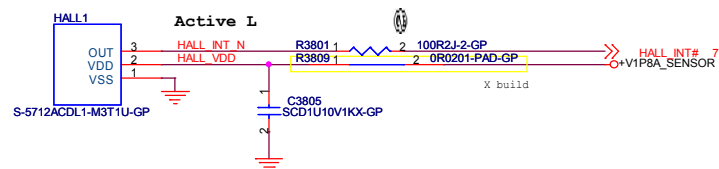
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Title 37_Thermal Protect			
Size A3	Document Number SILVERTON/SILVEROAK		Rev 2
Date: Saturday, July 19, 2014		Sheet 37	of 61

# Sensor

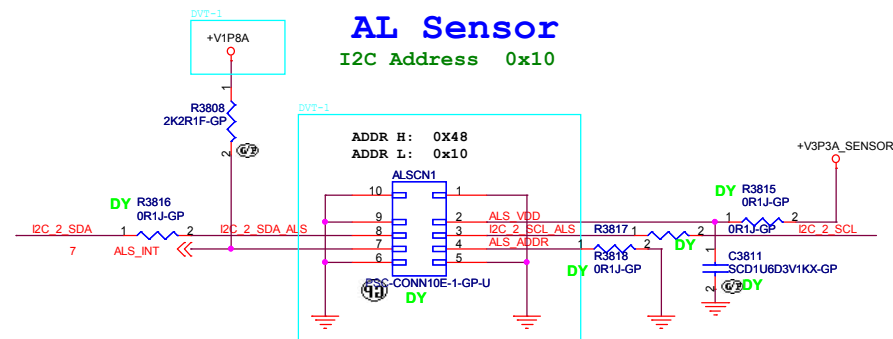


## HALL Sensor



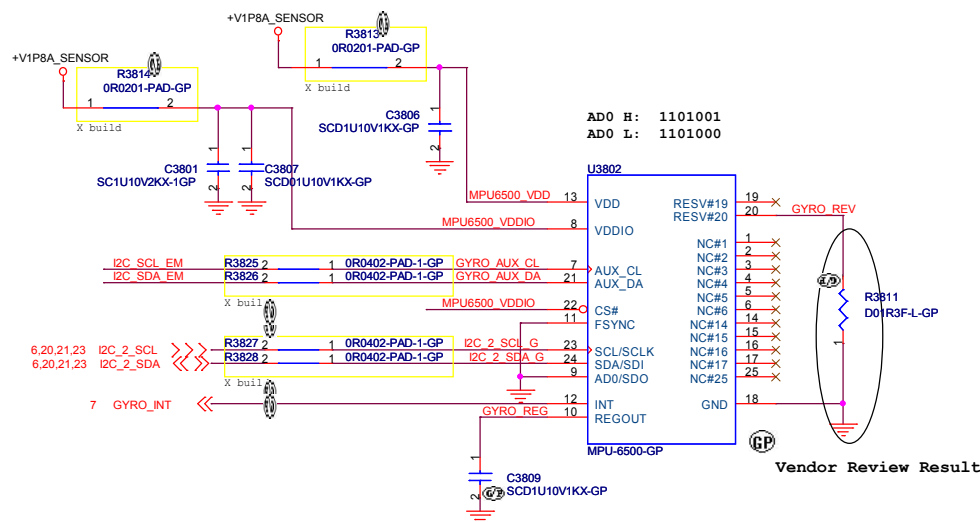
## AL Sensor

I2C Address 0x10



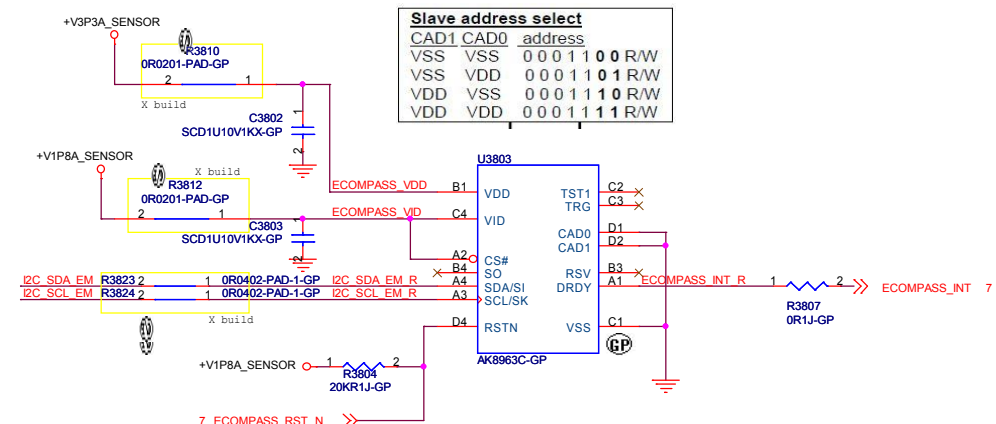
## G + Gyro Sensor

I2C Address 1101000



## E-Compass

I2C Address 0x0C

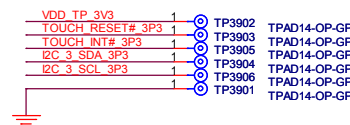
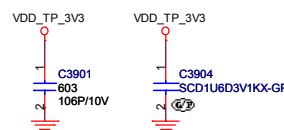
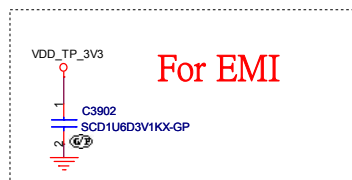
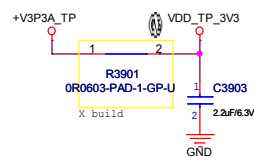
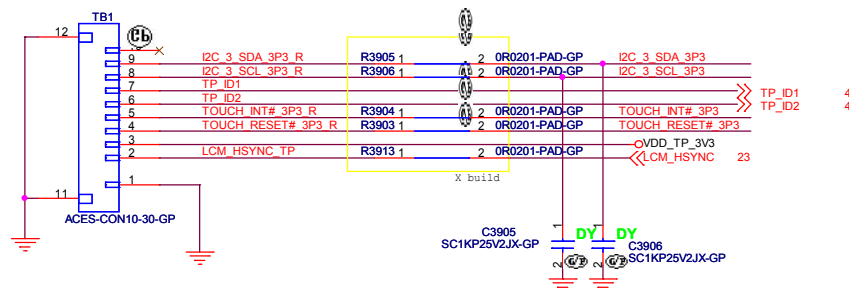


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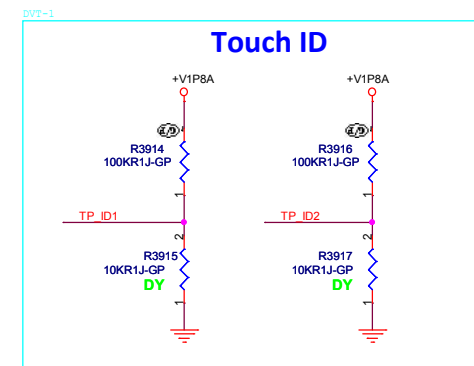
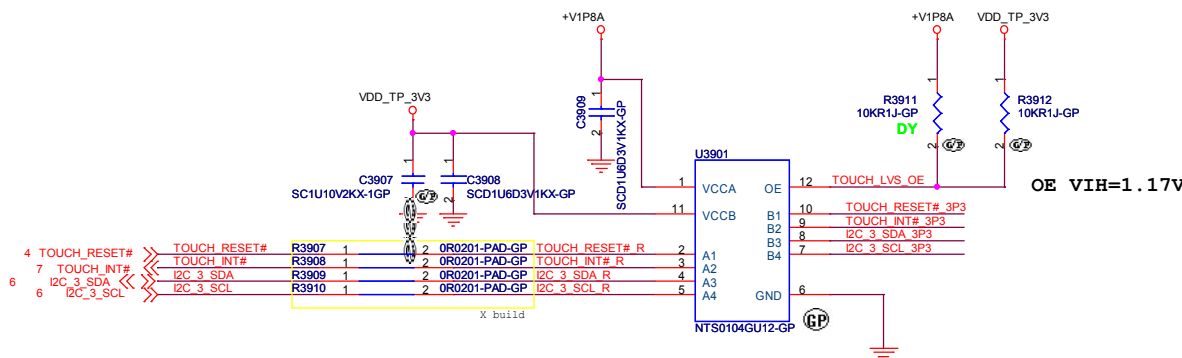
Title	38_Sensor	
Size	Document Number	Rev
A3	SILVERTON/SILVEROAK	0
Date:	Tuesday, December 09, 2014	Sheet 38 of 61

# Touch Panel



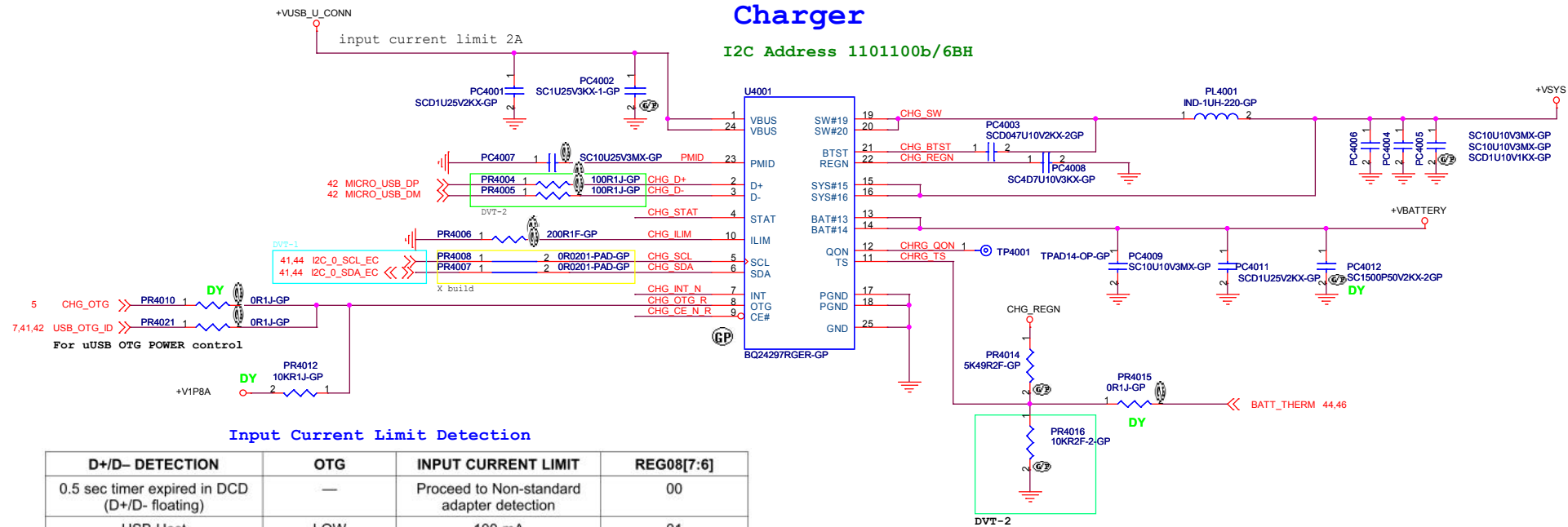
CN1 PIN #	Host 接續時	Description
1	NC	Keep Open
2	SDA	IIC Data Open drain; pull-up resistor at Host is needed
3	SCL	IIC Clock Open drain; pull-up resistor at Host is needed
4	ID01	Touch Sensor Identification Pin 01
5	ID02	Touch Sensor Identification Pin 02
6	IRQ	IIC Data Ready Output "LOW" when data ready to send Open drain; pull-up resistor at Host is needed
7	RESET	RESET Stop operation when pull "LOW" Build-in pull-up resistor 100kohm
8	VDD +3.3V	3.3volt power input
9	HSYNC	LCD Hsync input
10	GND	Ground

	ID1 (Pin 4)	ID2 (Pin 5)
HH	NC	NC
TPK	NC	GND
O-Film	GND	NC
Option2	GND	GND

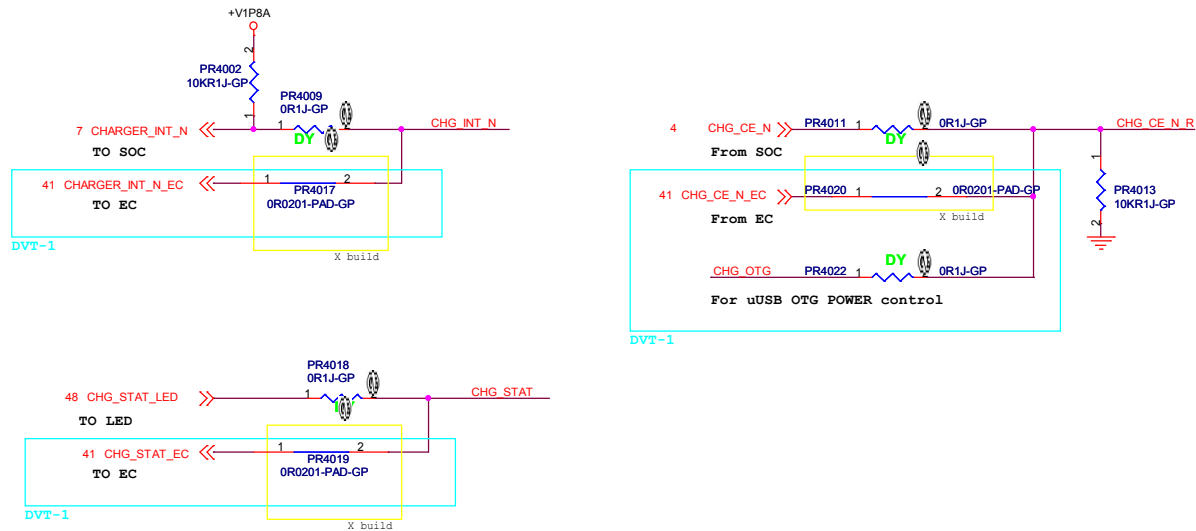


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## Charger

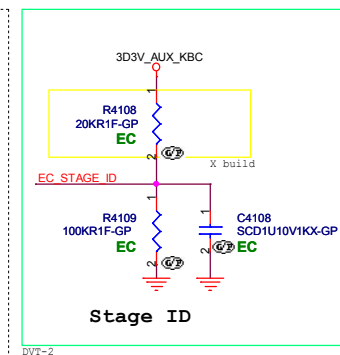


D+/D- DETECTION	OTG	INPUT CURRENT LIMIT	REG08[7:6]
0.5 sec timer expired in DCD (D+/D- floating)	—	Proceed to Non-standard adapter detection	00
USB Host	LOW	100 mA	01
USB Host	HIGH	500 mA	01
Charging Port	—	3 A	10



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PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage
DVT-2	100.0 K	10.0 K	3.000 V
X-build	100.0 K	20.0 K	2.750 V
Reserved for project use	100.0 K	33.0 K	2.481 V
Reserved for project use	100.0 K	47.0 K	2.245 V
Reserved for project use	100.0 K	64.9 K	2.001 V
Reserved for project use	100.0 K	76.8 K	1.867 V
Reserved for project use	100.0 K	100.0 K	1.650 V
Reserved for project use	100.0 K	143.0 K	1.358 V
Reserved for project use	100.0 K	174.0 K	1.204 V
Reserved for project use	100.0 K	215.0 K	1.048 V

# USB PHY

# USB MUX

The diagram illustrates the internal circuitry of a Micro USB connector, divided into two main sections: the top section for standard USB connections and the bottom section for Micro USB connections.

**Top Section (Standard USB):**

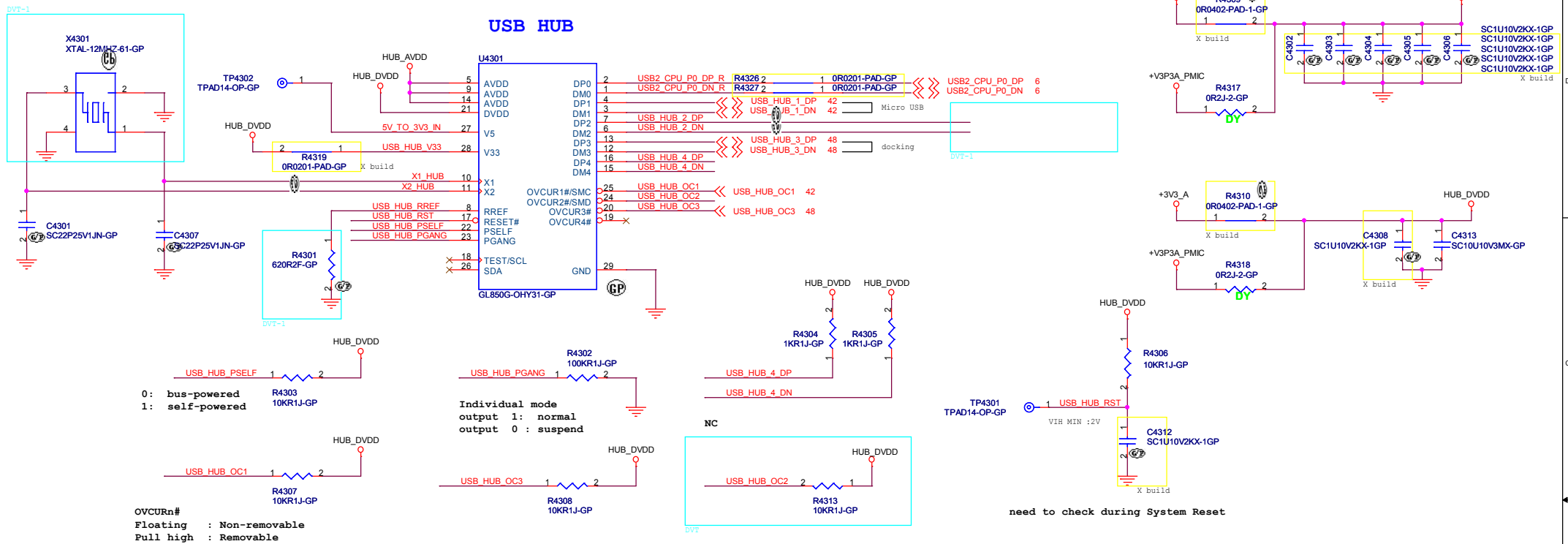
- Power Path:** +VSP1\_BOOST is connected to a network of capacitors (C4215, C4216, C4217) and resistors (R4219, R4220, R4221, R4222) to regulate the +VUSB\_U\_CONN signal.
- Current Limiting:** A current limit circuit (L4204) is used to protect the +VUSB\_U\_OTG\_OUT line, with a note indicating "Current Limit 1.5A".
- Signal Path:** The USB\_OTG\_EN signal is connected to a network of capacitors (C4215, C4216, C4217) and resistors (R4219, R4220, R4221, R4222) to regulate the +VUSB\_U\_CONN signal.
- Protection:** A varistor (V4202) is connected to the +VUSB\_U\_CONN line for surge protection.

**Bottom Section (Micro USB):**

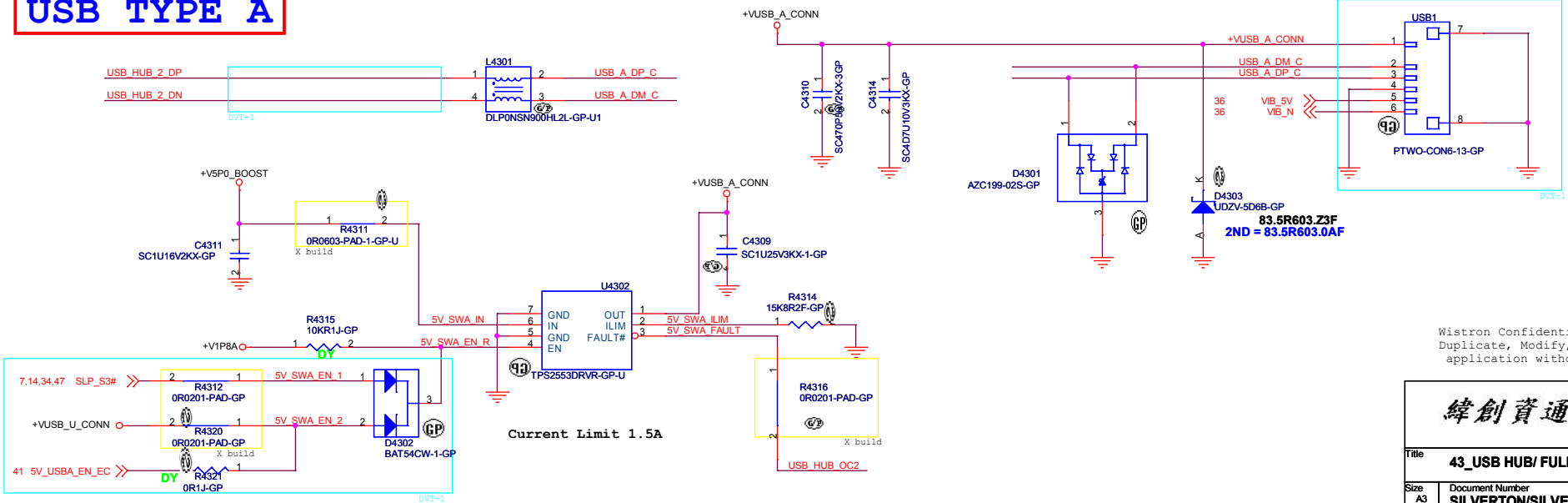
- Power Path:** +VUSB\_U\_CONN is connected to a network of capacitors (C4213, C4214, C4215, C4216, C4217) and resistors (R4219, R4220, R4221, R4222) to regulate the +VUSB\_U\_CONN signal.
- Signal Path:** The MICRO\_USB\_DP and MICRO\_USB\_DM signals are connected to a network of capacitors (C4213, C4214, C4215, C4216, C4217) and resistors (R4219, R4220, R4221, R4222) to regulate the +VUSB\_U\_CONN signal.
- Protection:** A varistor (V4202) is connected to the +VUSB\_U\_CONN line for surge protection.

**Micro USB Connector:** The diagram shows the physical connector pins (1-11) and their corresponding internal connections to the circuit components.

## USB HUB



## USB TYPE A



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Title	<b>43 USB HUB/ FULL USB CONN</b>
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Size A3	Document Number <b>SILVERTON/SILVEROAK</b>
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Date: Tuesday, December 09, 2014

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## FUEL GAUGE

# DVT-1

Pin #	Signal	Description/Function	Color
8	BATT+	Power, Batt +, Positive terminal of battery stack	RED
7	BATT+	Power, Batt +, Positive terminal of battery stack	RED
6	BATT+	Power, Batt +, Positive terminal of battery stack	RED
5	ID	Resistance TBD	BLUE
4	TS	Thermistor 103AT to the ground	YELLOW
3	GND	Power, Batt -, Negative terminal of battery stack	BLACK
2	GND	Power, Batt -, Negative terminal of battery stack	BLACK
1	GND	Power, Batt -, Negative terminal of battery stack	BLACK

```
Battery ID (PU 200K)
vendor 1: floating
vendor 2:PULL LOW with 10K
```

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Title	<b>44_BATT CONN</b>
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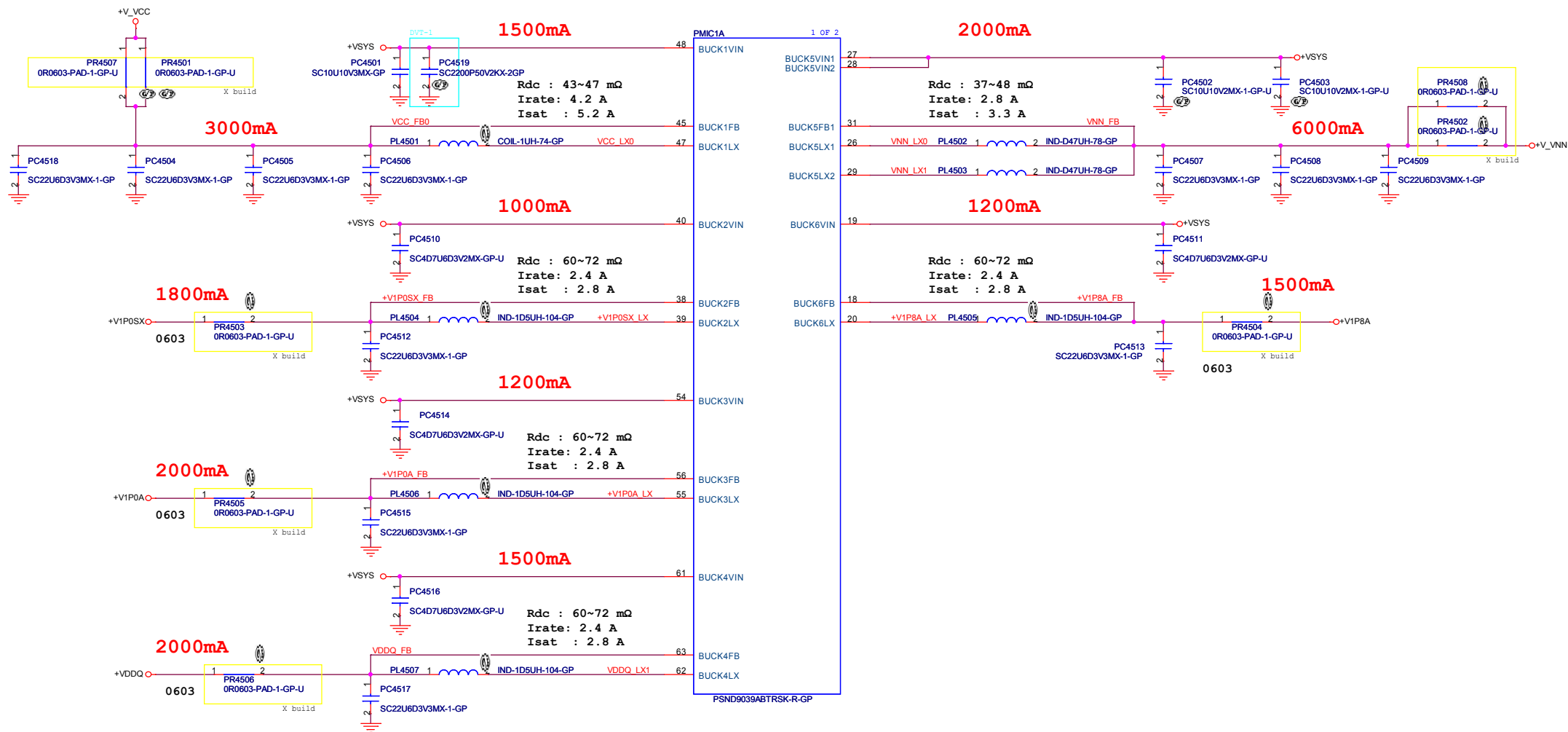
Size A3	Document Number <b>SILVERTON/SILVEROAK</b>
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Date: Tuesday, December 09, 2014



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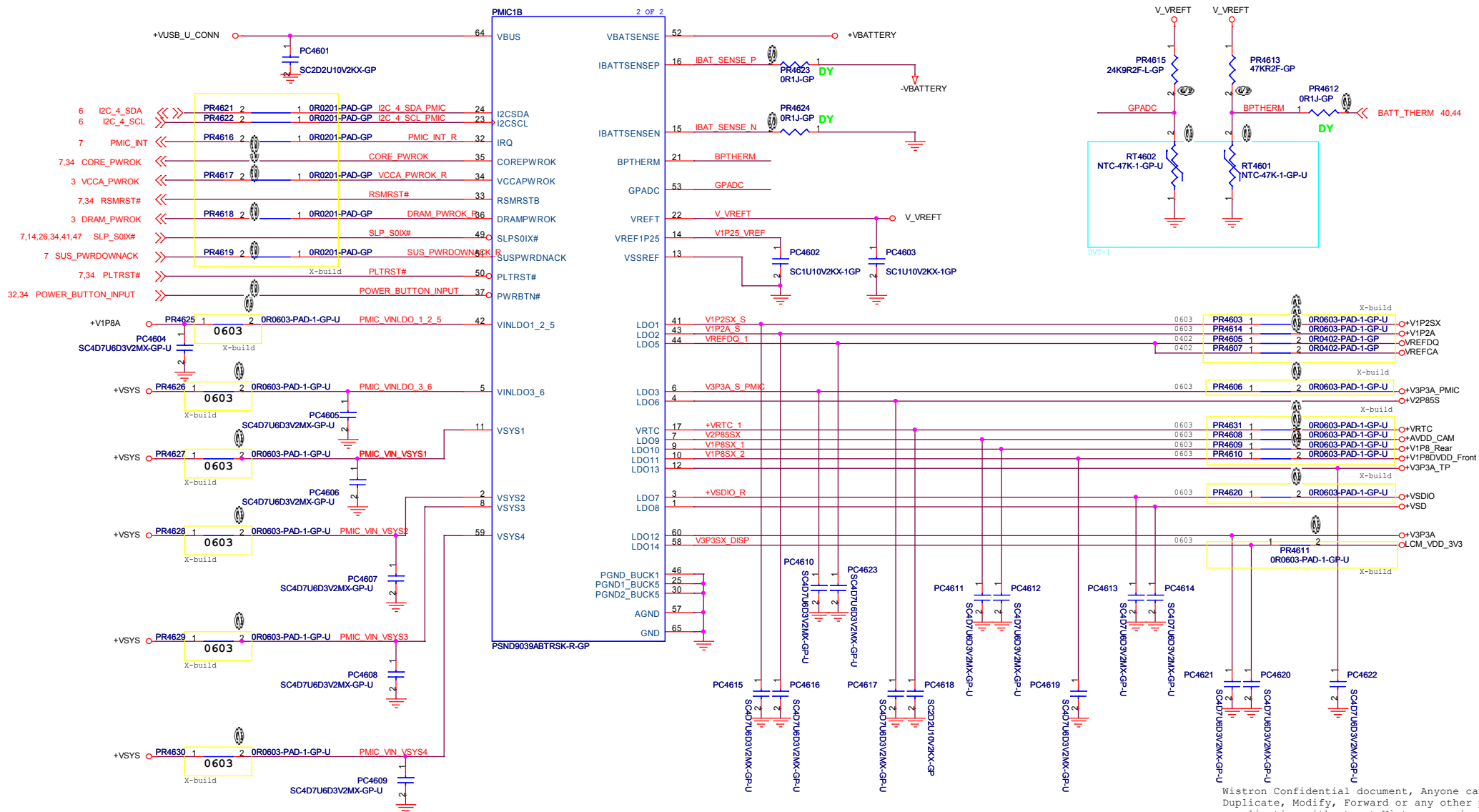
1

# PMIC : BUCK



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Title 45_PMIC(1/2)			
Size A3	Document Number SILVERTON/SILVEROAK		Rev 0
Date: Thursday, December 04, 2014	Sheet 45	of 61	

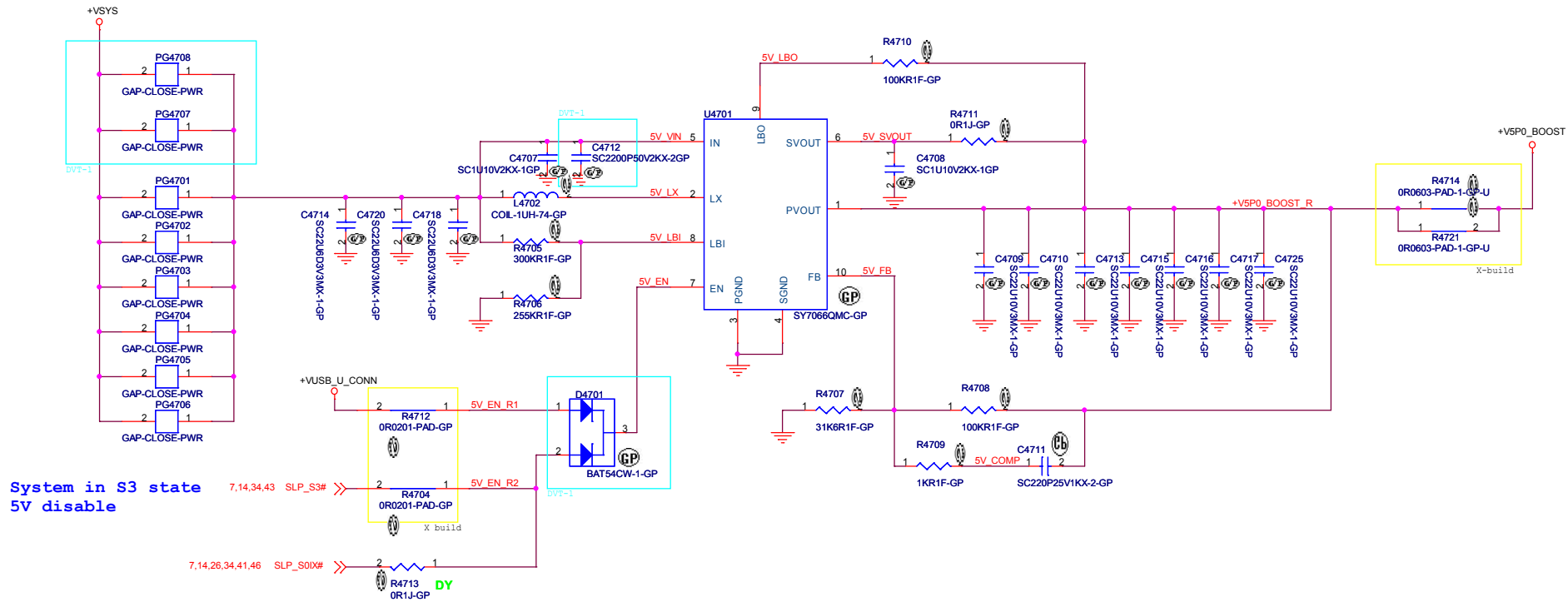


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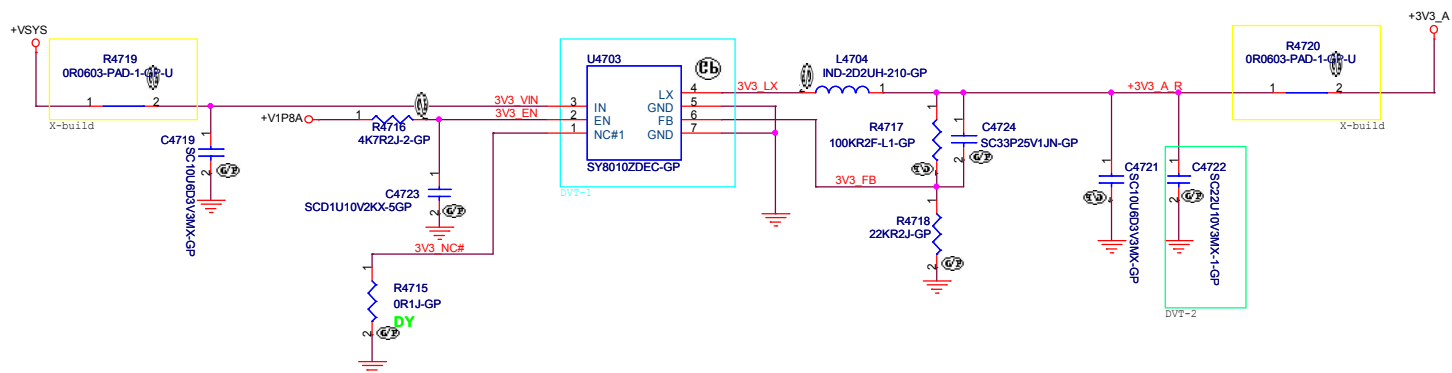
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Title			
46_PMIC(2/2)			
Size	Document Number	Rev	
A3	SILVERTON/SILVEROAK	0	
Date:	Tuesday, December 09, 2014	Sheet	46 of 61

5V BOOST 1 for HDMI / USB / LED /Audio AMP



## 3V3 BUCK for WIFI



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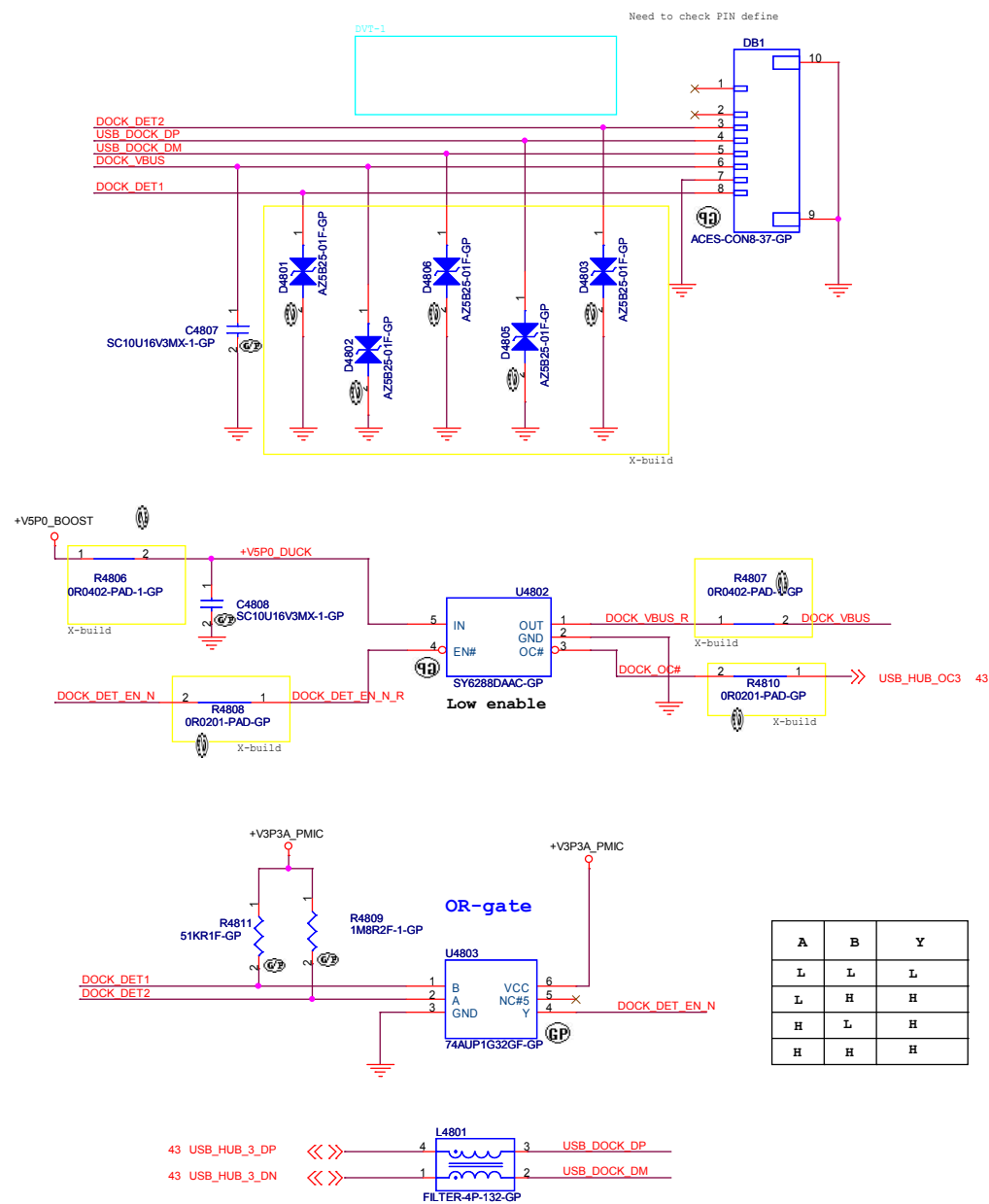
Title	<b>47_5V_BOOST &amp; 3.3V</b>
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Size A3	Document Number <b>SILVERTON/SILVEROAK</b>
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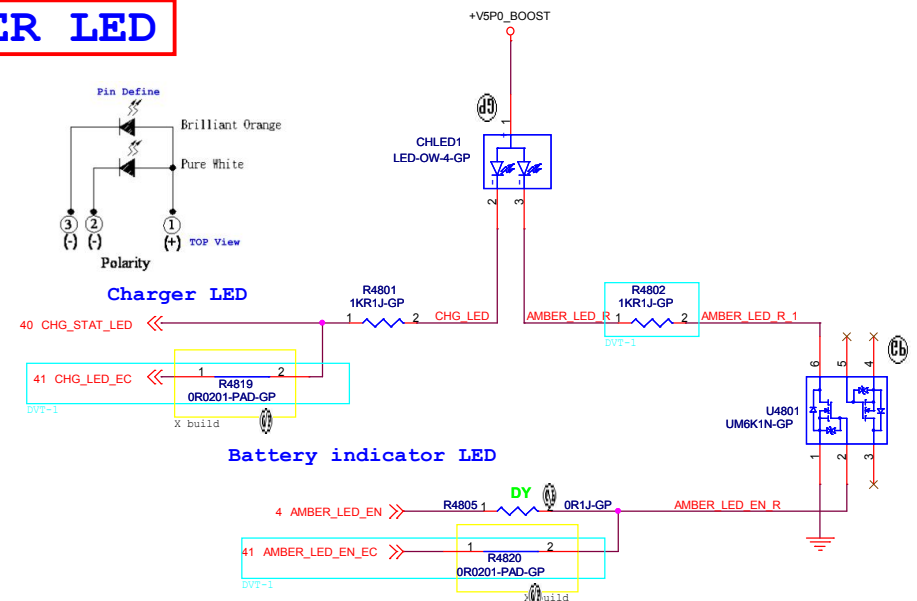
Date: Tuesday, December 09, 2014 Sheet 47 of 61

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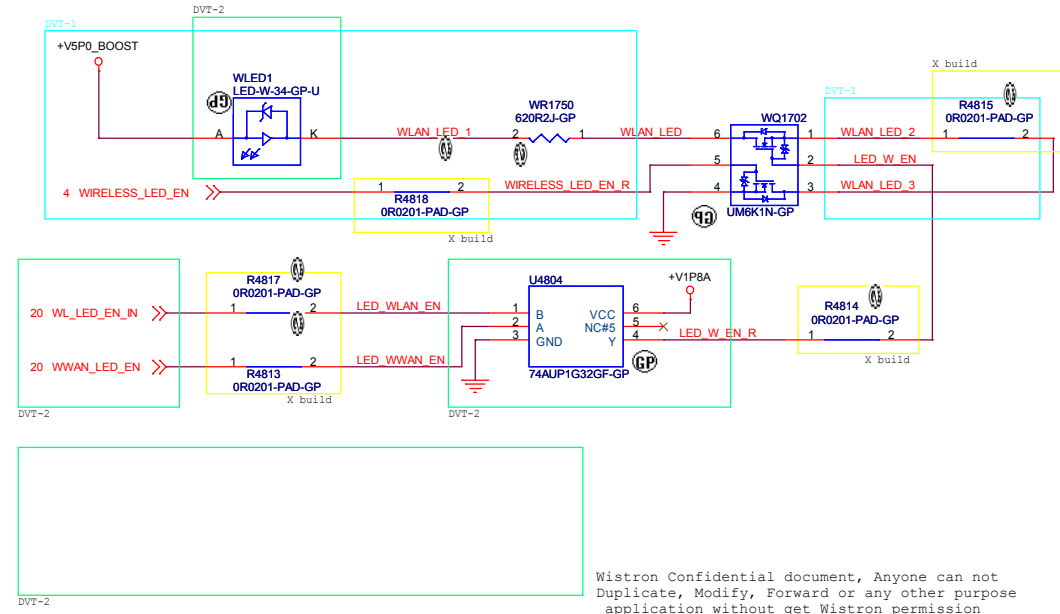
## Docking CONN



## POWER LED



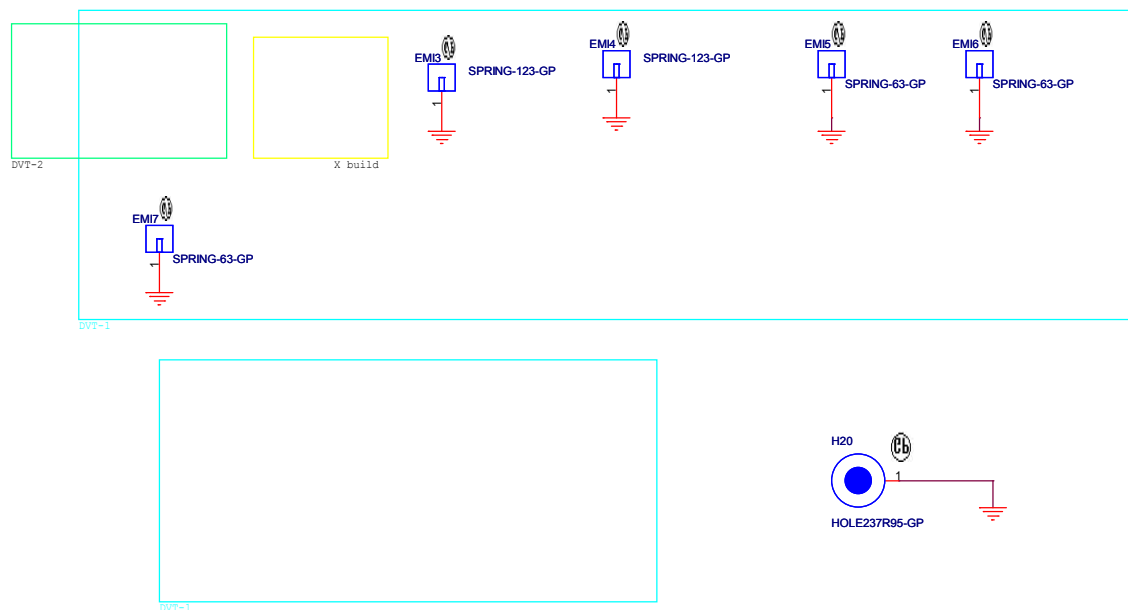
## WIRELESS LED



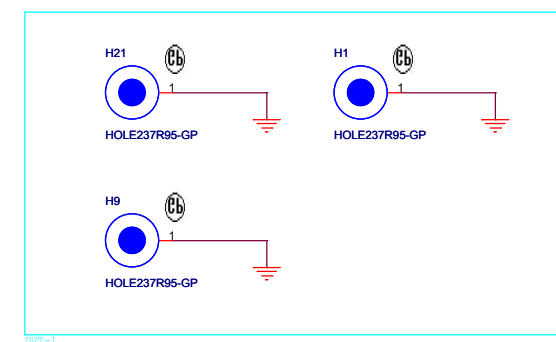
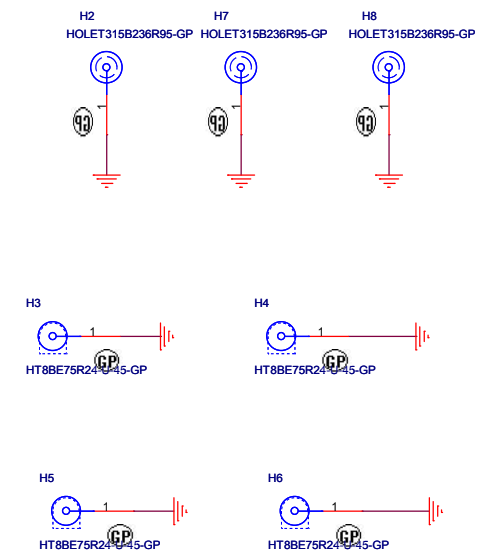
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## Shielding Can



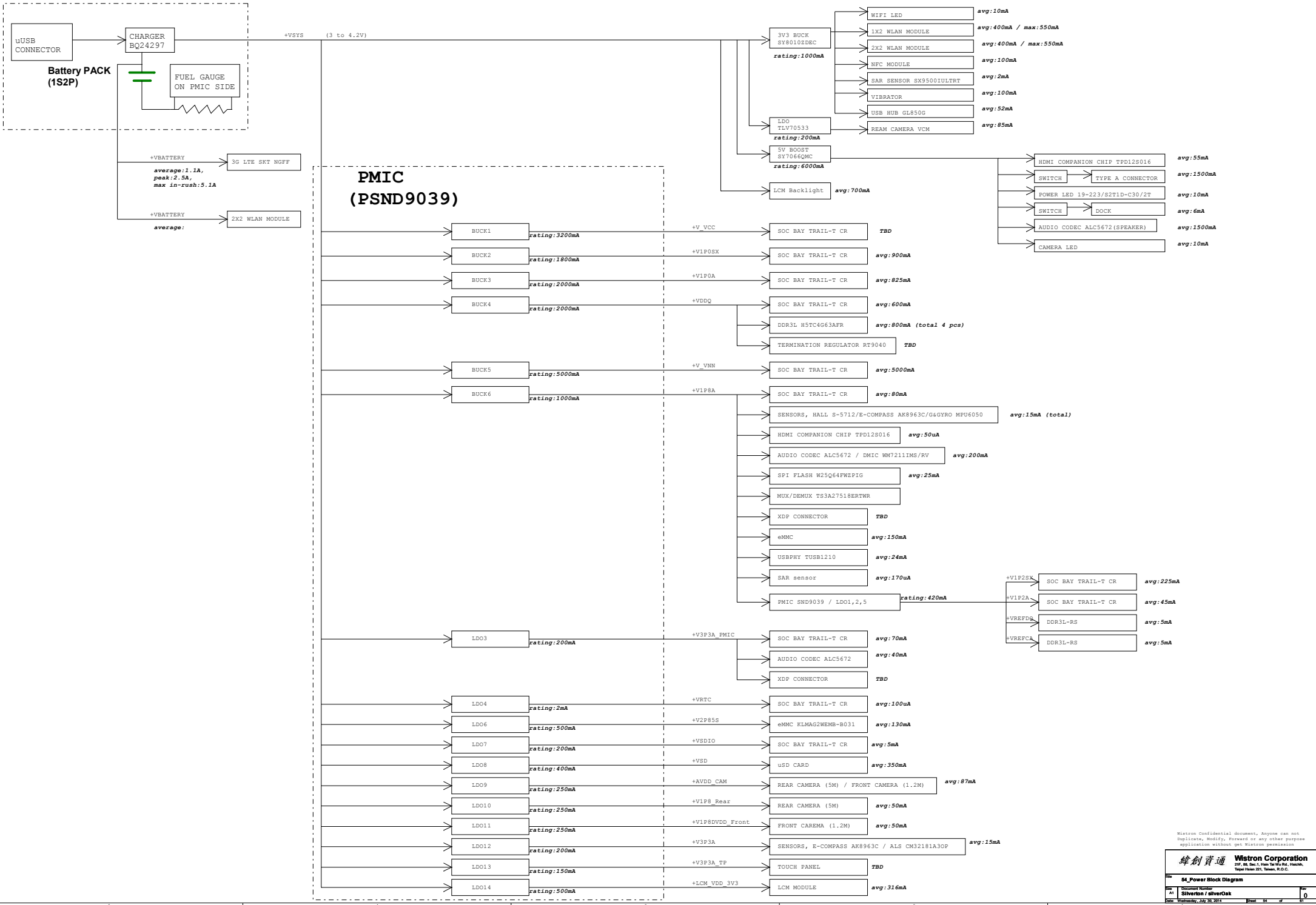
## Screw Hole

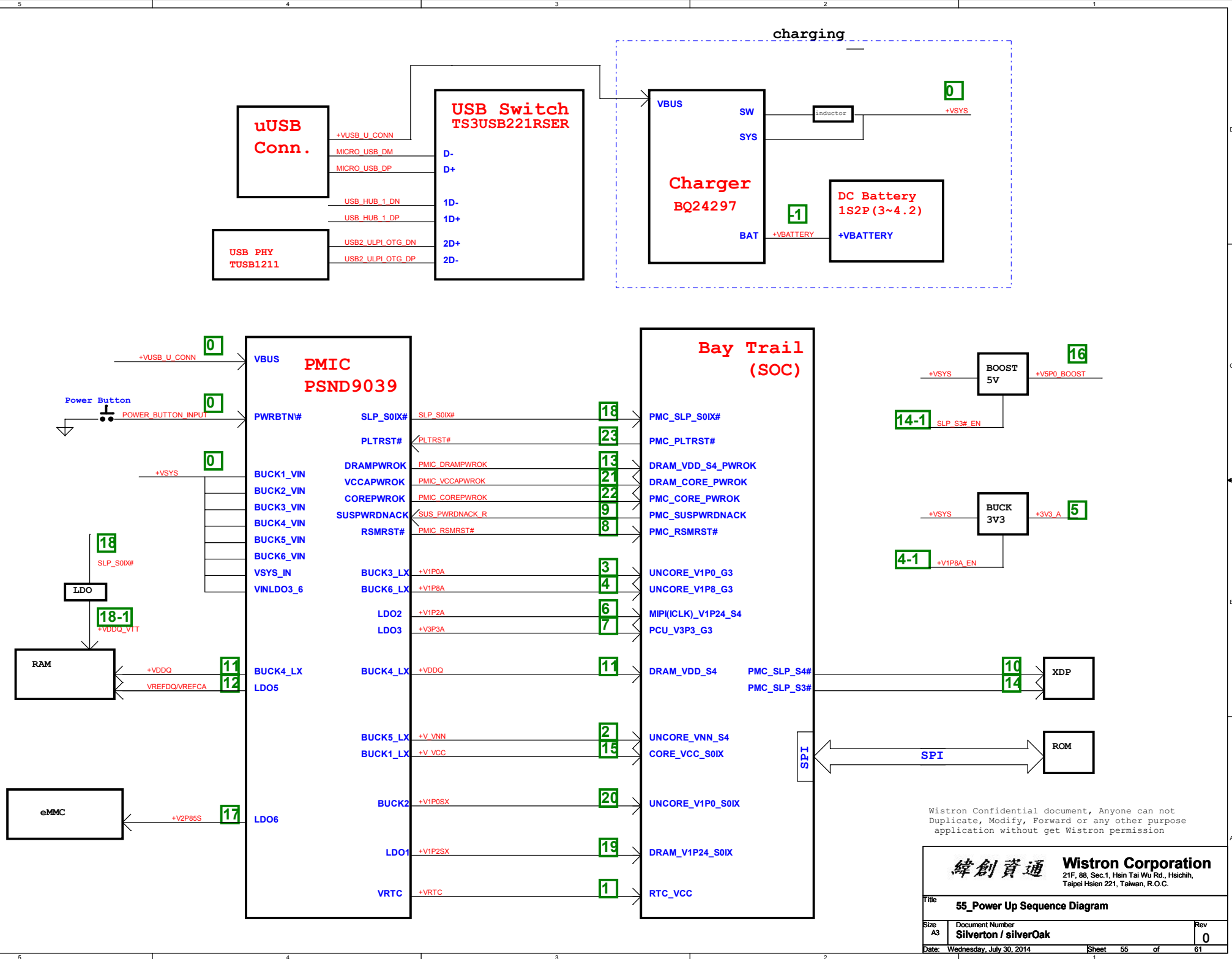


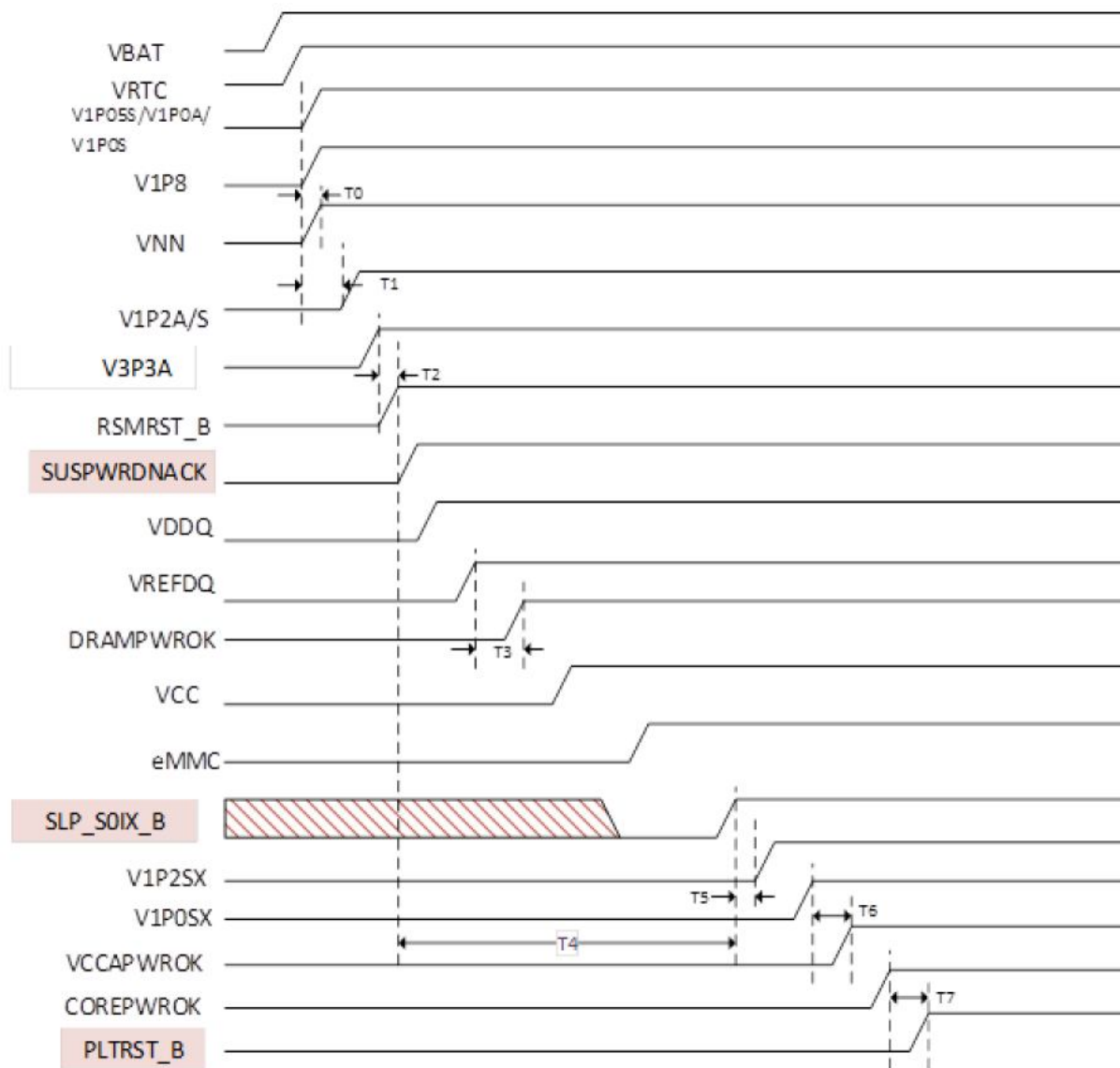
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Title: <b>53_ME/EMI</b>		
Size: <b>A3</b>	Document Number: <b>SILVERTON/SILVEROAK</b>	Rev: <b>0</b>
Date: <b>Monday, December 08, 2014</b>	Sheet: <b>53</b>	of: <b>61</b>

# BAYTRAIL T-CR POWERMAP



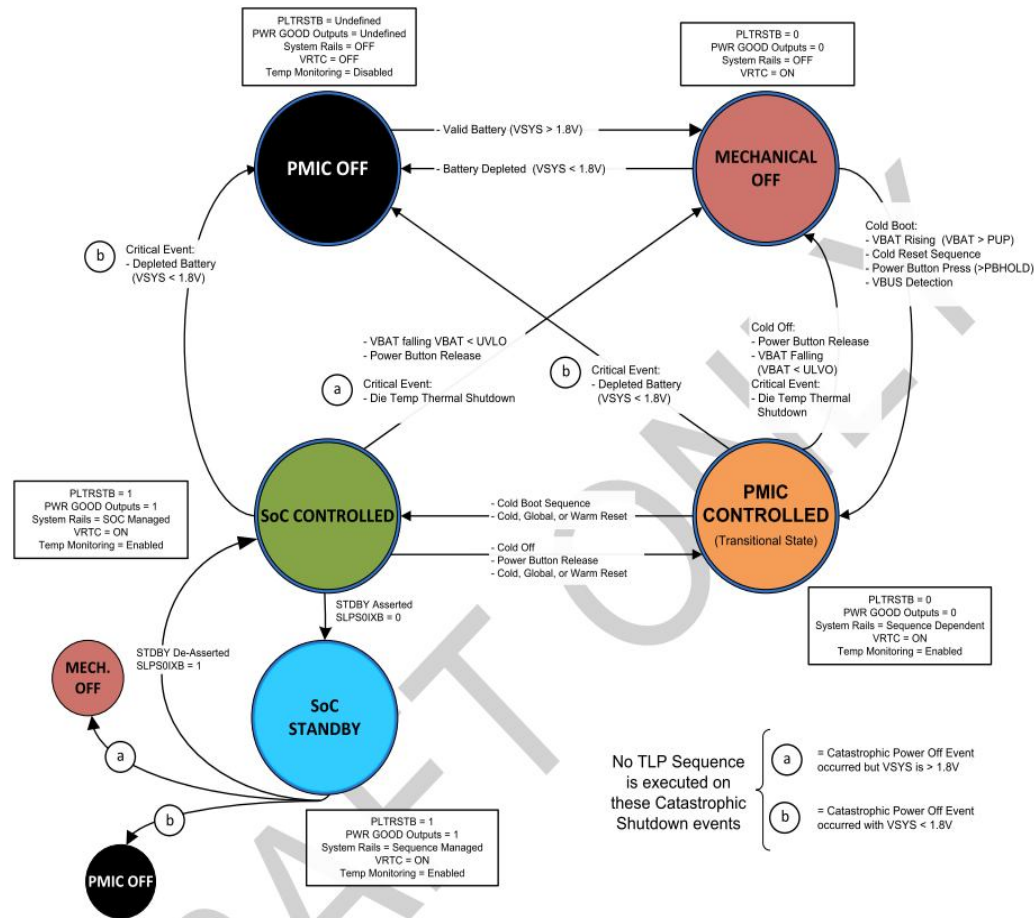




Parameter	Description	Min	Typical	Max	Unit
T0	Rail Ramp-Up Time from 10% to 90% voltage level	0.08	1	2	ms
T1	Rail to Subsequent Rail Turn-On Delay	0.5	1	2.05	ms
T2	V3P3A valid to RSMRST_B de-assertion	0		150	us
T3	VREFDQ valid (within +/-10% of its final normal value) to DRAMPWROK assertion	0		150	us
T4	RSMRST_B de-assertion to SLP_SOIX_B de-assertion	80			us
T5	SLP_SOIX_B de-assertion to first SX rail turn-on delay	0	8	16	ms
T6	Core rails valid to VCCAPWROK and COREPWROK assertion		1		ms
T7	COREPWROK assertion to PLTRST_B de-assertion	60			us

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Title <b>57_Power Sequence Timing</b>		
Size A3	Document Number <b>Silverton / silverOak</b>	Rev <b>0</b>
Date: Wednesday, July 30, 2014 Sheet 56 of 61		



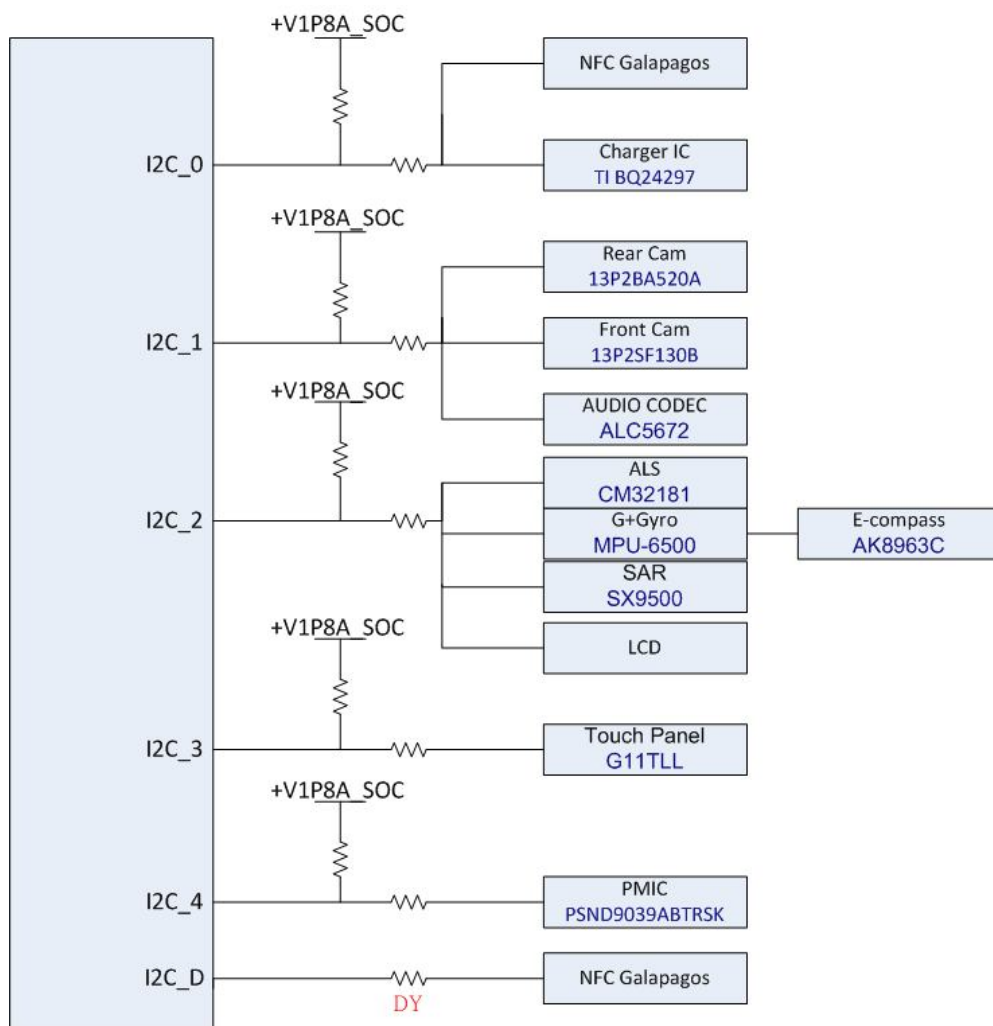
	PART	BUCK1	BUCK2	BUCK3	BUCK4	BUCK5	BUCK6	LD01	LD02	LD03	VRTC	LD04	VREFDQ	LD05	LD06	LD07	LD08	LD09	LD010	LD011	LD012	LD013	LD014	Comment
PMIC OFF	BYT	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
	CHT	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
Mechanical Off	BYT	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
	CHT	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
SoC Control led	BYT	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	Disabled by default. SoC can enable/disable according to system activity							VREFT can be turned on and off for thermistor and GPADC biasing	
	CHT	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	Disabled by default. SoC can enable/disable according to system activity								
SoC Stand-by	BYT	OFF	OFF	ON	V <sub>SLEEP</sub>	ON	V <sub>SLEEP</sub>	ON	ON	ON	ON	ON	ON	ON	ON	Will keep whatever state had before entering standby							I2C is operational VREFT can be turned on and off for thermistor and GPADC biasing	
	CHT	OFF	ON	V <sub>SLEEP</sub>	V <sub>SLEEP</sub>	ON	OFF	ON	ON	ON	ON	ON	ON	ON	ON	Will keep whatever state had before entering standby								

LD07-LD014 will keep whatever state before entering standby, it's up to the user whether to enable/disable. State machine won't enforce the behavior in this case.

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Title <b>57_Power State</b>	
Size A3	Document Number <b>Silverton / silverOak</b>
Date: Wednesday, July 30, 2014	Rev <b>0</b>
Sheet 57	of 61

# I2C Block Diagram

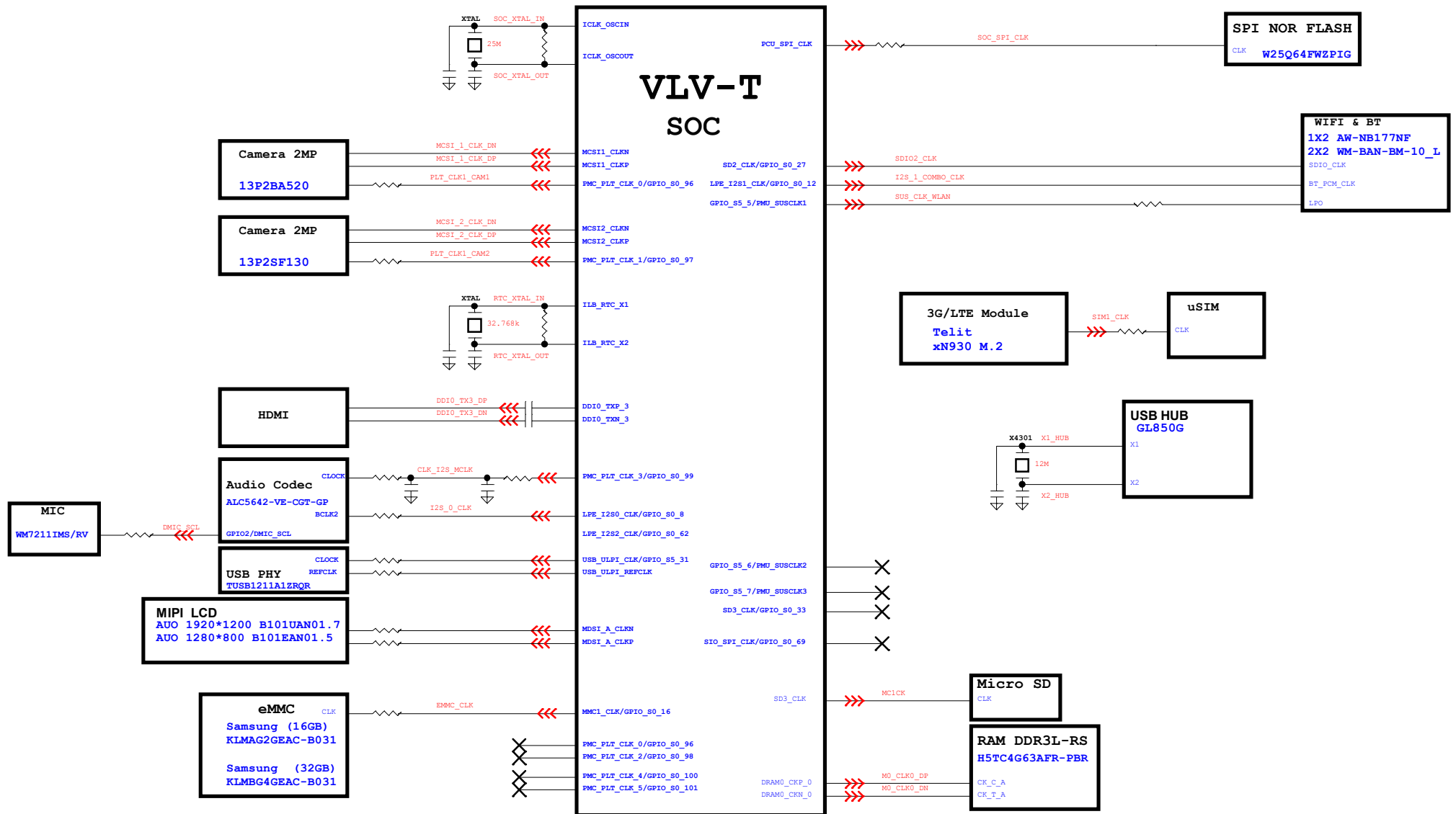


I2C	Function	Device	address (7-bits)
0	Charger IC	BQ24297	6BH
	NFC	Galapagos	29H
1	Audio Codec	ALC5672	1CH
	Front Cam	MI1040	48H
	Rear Cam	OV5693	10H
	Rear Cam VCM	AD5823BCDZ	18H
2	LCD		
	ALS	CM32181	10H
	E-compass	AK8963C	0CH
	G+Gyro	MPU-6500	68H
	GNSS		
	SAR	SX9500	28H
3	Touch IC	G11TLL	
4	PMIC	PSND9039	05E
D1	NFC	Galapagos	29H

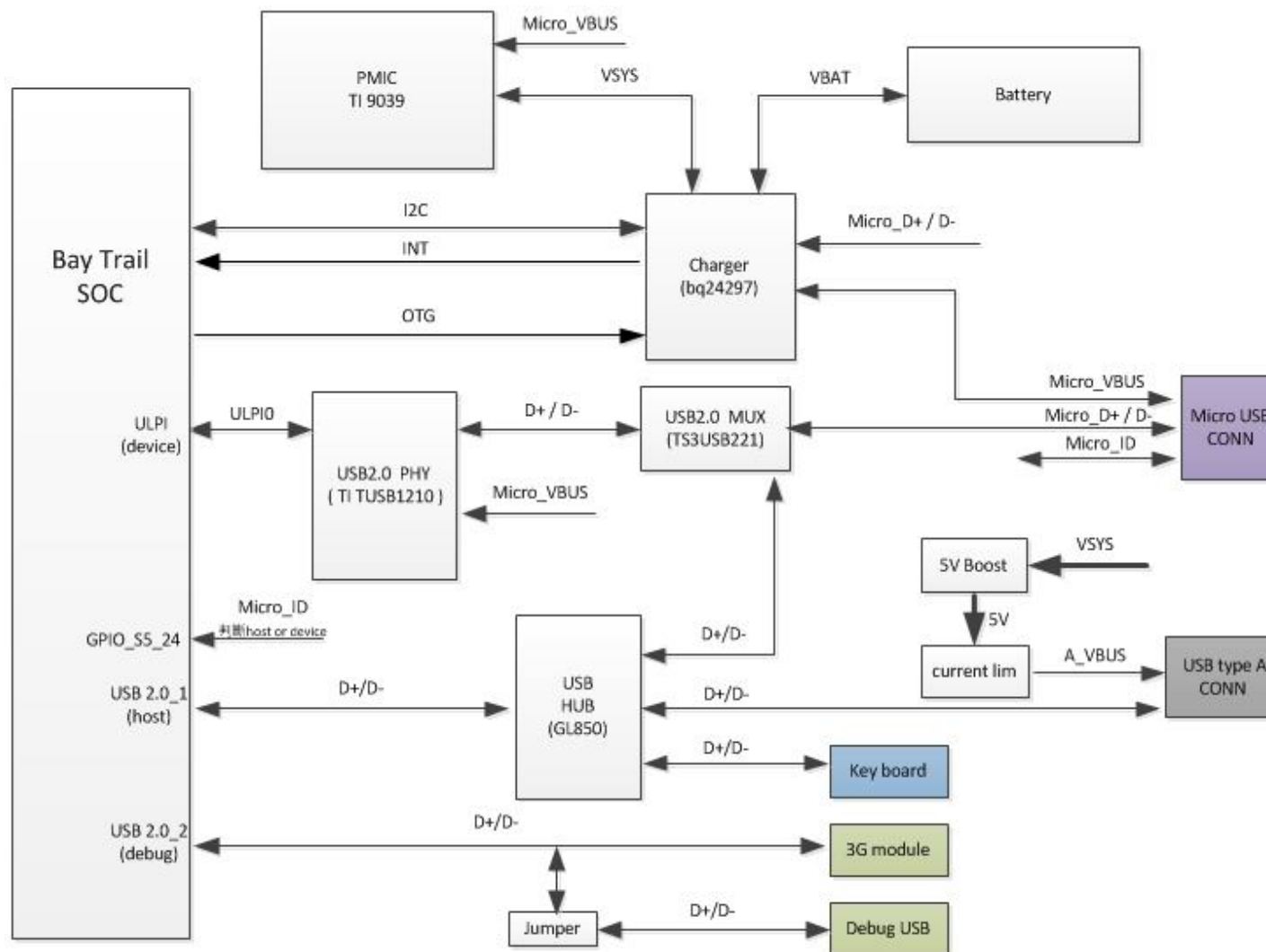
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Title <b>58_I2C BLOCK DIAGRAM</b>	
Size A3	Document Number <b>Silverton / silverOak</b>
Date: Wednesday, July 30, 2014	Sheet 58 of 61
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# CLOCK Block Diagram



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Title **60\_USB IO BLOCK DIAGRAM**

Size A Document Number **SILVERTON/SILVEROAK**

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Date: Wednesday, July 30, 2014

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Title 61_Change History			
Size A3	Document Number SILVERTON/SILVEROAK		Rev 0
Date: Wednesday, July 30, 2014	Sheet 1	61 of	61